Talaria TWO™ (INP2045)

Ultra-Low Power Multi-Protocol Wireless Platform SoC

IEEE 802.11 b/g/n, BLE 5.0

Talaria TWO™ Module and SoC Datasheet

Application Product Numbers:

INP1010, INP1011, INP1012, INP1013, INP1014, INP1015 and INP2045 SoC

Date: 08-23-2023

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Revision History

Version	Date	Comments
1.0	05-15-2020	Internal Draft.
2.0	06-30-2020	Initial Publication.
2.1	07-10-2020	Storage Conditions. Storage period changed to 12months from 6 month.
2.2	07-29-2020	802.11g Output Power changed to 15.5dBm from 15.0dBm. 802.11n Output Power changed to 12.5dBm from 13.0dBm.
2.3	08-11-2020	Currents updated with 3-lot data.
2.4	09-1-2020	Inserted Advanced Security Elements Updated Wi-Fi EVM and Rx Sensitivity in Section 16 Updated INP1010 & INP1011 Ordering Part Numbers
3.0	01-15-2021	Updates to add INP1012 and INP1013 mini modules. Included SPI Master details. Updated Peripheral Signal Mapping table.
3.1	02-20-2021	Added INP1012 Schematic Added antenna dimensions on INP1013 dimensions GPIO LOW for lowest power Sleep Mode added in note
4.0	05-06-2021	Add sections supporting INP2045 Chip. Updated module schematics.
5.0	11-30-2021	Add INP1014 and INP1015 module information Added SDIO peripheral information Updated with BLE RF Data.
6.0	06-09-2022	Updated to remove channel 14 mentions since Talaria TWO does not support operation in this channel. Added TELEC certification. Increased max. Input Supply Current to 500mA. Set Sleep Mode Current to 19uA.
6.1	06-21-2022	Amended ADC details to state 12-bit (10-bit effective). Added clarification that VDDIO is an output.
6.2	06-29-2022	Updated center ground pads numbering on Section 11 Module Pin-Out diagrams and table. Updated UART baud-rate max to 921600.
6.3	07-14-2022	Removed “Connect to Pin 24” from Pin 41– INP2045 SoC Pin Descriptions.
7.0	09-02-2022	Updated DC & RF Characteristics of Wi-Fi 802.11b 2.4GHz, Wi-Fi 802.11g 2.4GHz and Wi-Fi 802.11n 2.4GHz.

8.0	08-01-2023	Updated to include a note on GPIO19 functioning in Peripheral Signal Mapping section.
8.1	08-23-2023	Updated: - To include a note on static caution warning in the Overview section. - INPI014 and INP1015 module and EVB images.

Contents

Figures

Tables

Terms & Definition

ADC	Analog to Digital Convertor
BLE	Bluetooth Low Energy
DMA	Direct Memory Access
EVM	Error Vector Magnitude
GAP	Generic Access Profile
GATT	Generic Attribute Profile
GPIO	General-Purpose Input/Output
HAPI	Host Application Programming Interface
JTAG	Joint Test Action Group
MCU	Microcontroller Unit
PHY	Physical Layer
RTC	Remote Time Clock
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver-Transmitter

Overview

The INP1010/INP1011/INP1012/INP1013/INP1014/INP1015 Talaria TWO modules are complete solutions with integrated wireless connectivity plus microcontroller for edge-of-network IoT designs. They use InnoPhase's award-winning Talaria TWO™ Multi-Protocol System on Chip (INP2045 SoC) with Wi-Fi and BLE5 for wireless data transfer, an embedded Arm Cortex-M3 for system control and user applications plus advanced security elements for device safeguards.

The Talaria TWO's unique digital polar radio architecture makes the modules the world's lowest power Wi-Fi solutions. It also provides BLE connectivity for Wi-Fi provisioning, diagnostics and other local communication. The integrated solution is ideally suited for battery-based, direct-to-cloud devices such as smart door locks, remote security cameras and connected sensors.

The Talaria TWO modules have either a printed PCB antenna (INP1010/INP1014), a U.FL antenna connector (INP1011/INP1015), an RF pin connector (INP1012), or a ceramic antenna (INP1013). The modules will include Wi-Fi Alliance, Bluetooth SIG, FCC, IC (Canada), CE, and TELEC*. Each module has an associated EVB-A evaluation board (INP3010/INP3011/INP3012/INP3013/INP3014/INP3015 respectively) – see the Talaria TWO EVB-A User Guide available at innophaseiot.com/talaria-two-modules/ for more information.

Note: Users must ensure to do their own EMC and safety assessment along with any RF spot checks as applicable while integrating Talaria TWO modules onto their application/Host/final product.

*Only for INP1014 and INP1015 modules

Module Images

INP1010

(w/PCB Antenna)

INP1011

(w/U.FL Connector)

INP1012

(w/RF Pad)

INP1013

(w/U.FL Connector)

INP1014

(w/PCB Antenna)

INP1015

(w/U.FL Connector)

Figure 1: INP101x modules

Evaluation Board Images

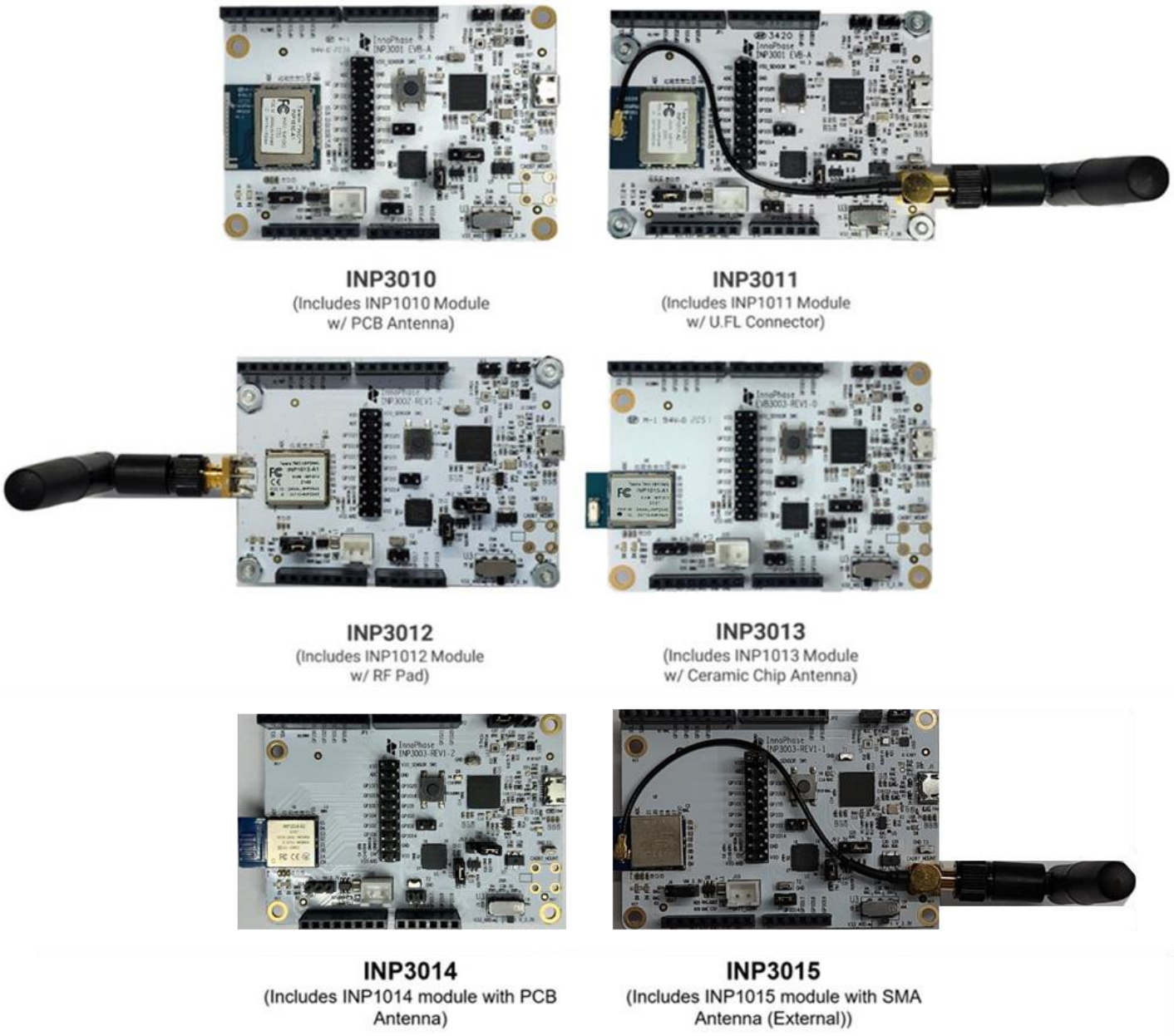


Figure 2: INP301x EVB-A Board with INP101x module board installed

Key Features

1. Ultra-low power 2.4GHz 802.11 b/g/n Wi-Fi connectivity
2. Support for WPA2 (Personal & Enterprise) and WPA3
3. DTIM10 at 57uA enables Wi-Fi connected battery-based applications
4. Full stack including MQTT, mbedTLS for supporting IoT Direct-to-Cloud for a variety of cloud services (AWS, Azure, Google Cloud, IBM Watson, etc.)
5. BLE5.0 w/ Advanced Features LE Coding/FEC (Long-Range), 2M PHY, Extended Advertising
6. Supports Wi-Fi Provisioning over BLE and local device management, plus BLE to Wi-Fi bridging
7. Bluetooth GATT/GAP Profile support, and HCI interface option for host MCU-based BLE profile stacks
8. Advanced security features including Secure Boot, PUF (Physically Unclonable Function) and hardware Crypto Engines
9. Embedded 80MHz Arm Cortex-M3 w/ 512KB SRAM and 2MB Flash
10. Host Interface over SPI or UART using InnoPhase HIO API (HAPI) C library or AT Commands
11. Eleven (11) configurable GPIO plus Tx Console port (on GPIO17)
12. Dedicated ADC Input pin
13. Integrated clocks and power management – only a single 3.3V supply needed
14. PCB antenna, U.FL antenna connector, RF Pin, and ceramic antenna options

Part Numbers and Revision History

Manufacturer Part Number	Revision	Description
INP1010	A1	Talaria TWO module, PCB Antenna, Production
	A2	Production, Hibernate Mode Enabled
INP1011	A2	Talaria TWO module, U.FL Antenna Connector, Production
	A3	Production, Hibernate Mode Enabled
INP1012	A1	Talaria TWO mini-module, RF Pin Antenna Connector, Production
INP1013	A1	Talaria TWO mini-module, Ceramic Antenna, Production
INP1014	A1	Talaria TWO mini-module, PCB Antenna, Production
INP1015	A1	Talaria TWO mini-module,U.FL Antenna Connector, Production
INP3010	A2	Evaluation Board (EVB-A) w/ INP1010 module, PCB Antenna (see separate User Guide for Talaria TWO EVB-A Evaluation Board for more information at innophaseiot.com/talaria-two-modules/#documentation-software)
INP3011	A2	Evaluation Board (EVB-A) w/ INP1011 module, U.FL Antenna Connector (see separate User Guide for Talaria TWO EVB-A Evaluation Board for more information at innophaseiot.com/talaria-two-modules/#documentation-software)
INP3012	A1	Evaluation Board (EVB-A) w/ INP1012 module, RF Pin Antenna Connector (see separate User Guide for Talaria TWO EVB-A Evaluation Board for more information at innophaseiot.com/talaria-two-modules/#documentation-software)
INP3013	A1	Evaluation Board (EVB-A) w/ INP1013 module, Ceramic Antenna (see separate User Guide for Talaria TWO EVB-A Evaluation Board for more information at innophaseiot.com/talaria-two-modules/#documentation-software)
INP3014	A1	Evaluation Board (EVB-A) w/ INP1014 module, PCB Antenna (see separate User Guide for Talaria TWO EVB-A Evaluation Board for more information at innophaseiot.com/talaria-two-modules/#documentation-software)
INP3015	A1	Evaluation Board (EVB-A) w/ INP1015 module, U.FL Antenna Connector (see separate User Guide for Talaria TWO EVB-A Evaluation Board for more information at innophaseiot.com/talaria-two-modules/#documentation-software)

Table 1: Part numbers with revision history

Module Dimensions

INP1010 and INP1011

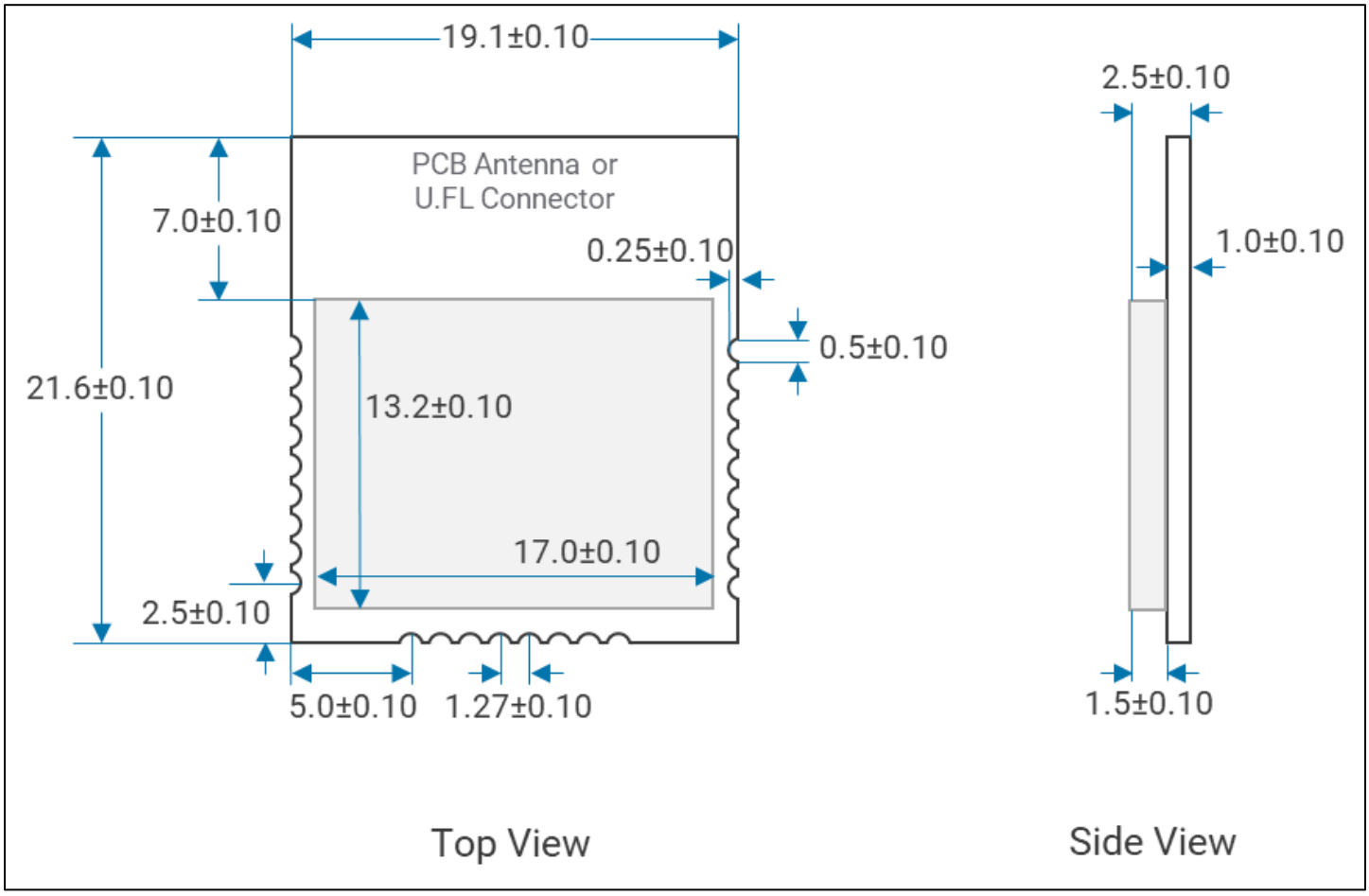


Figure 3: INP1010/11 module dimensions

INP1012

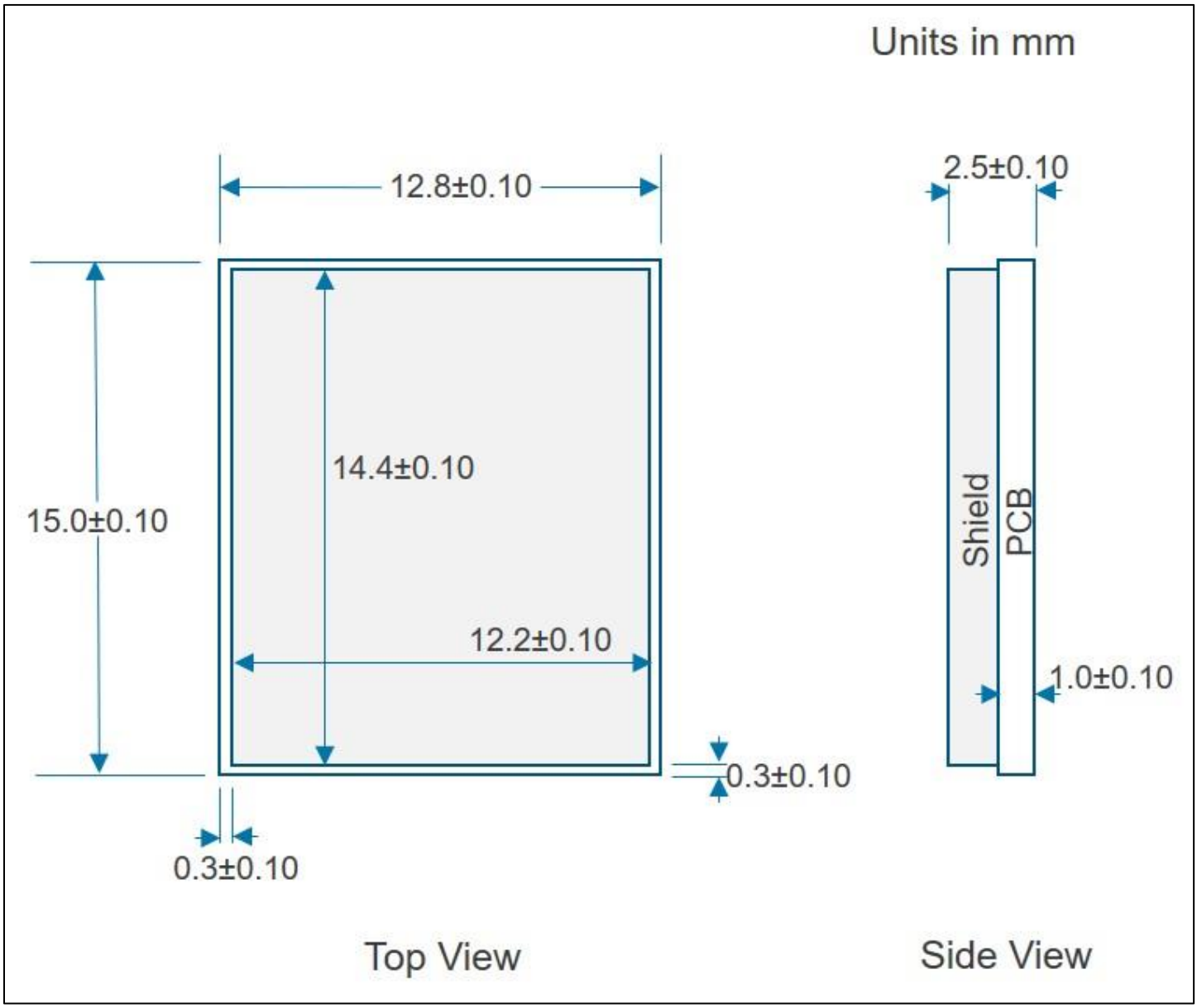


Figure 4: INP1012 module dimensions

INP1013

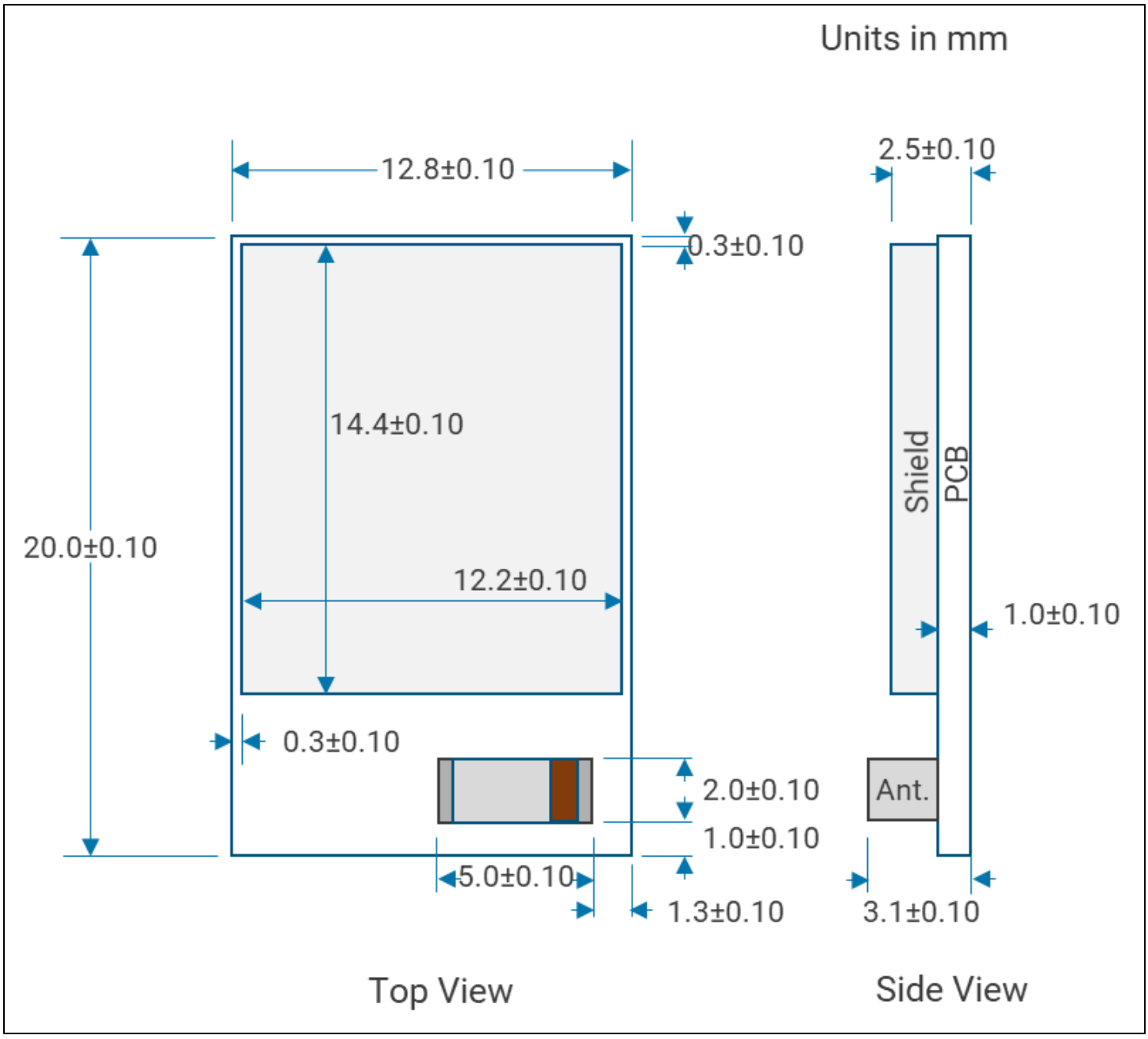


Figure 5: INP1013 module dimensions

INP1014

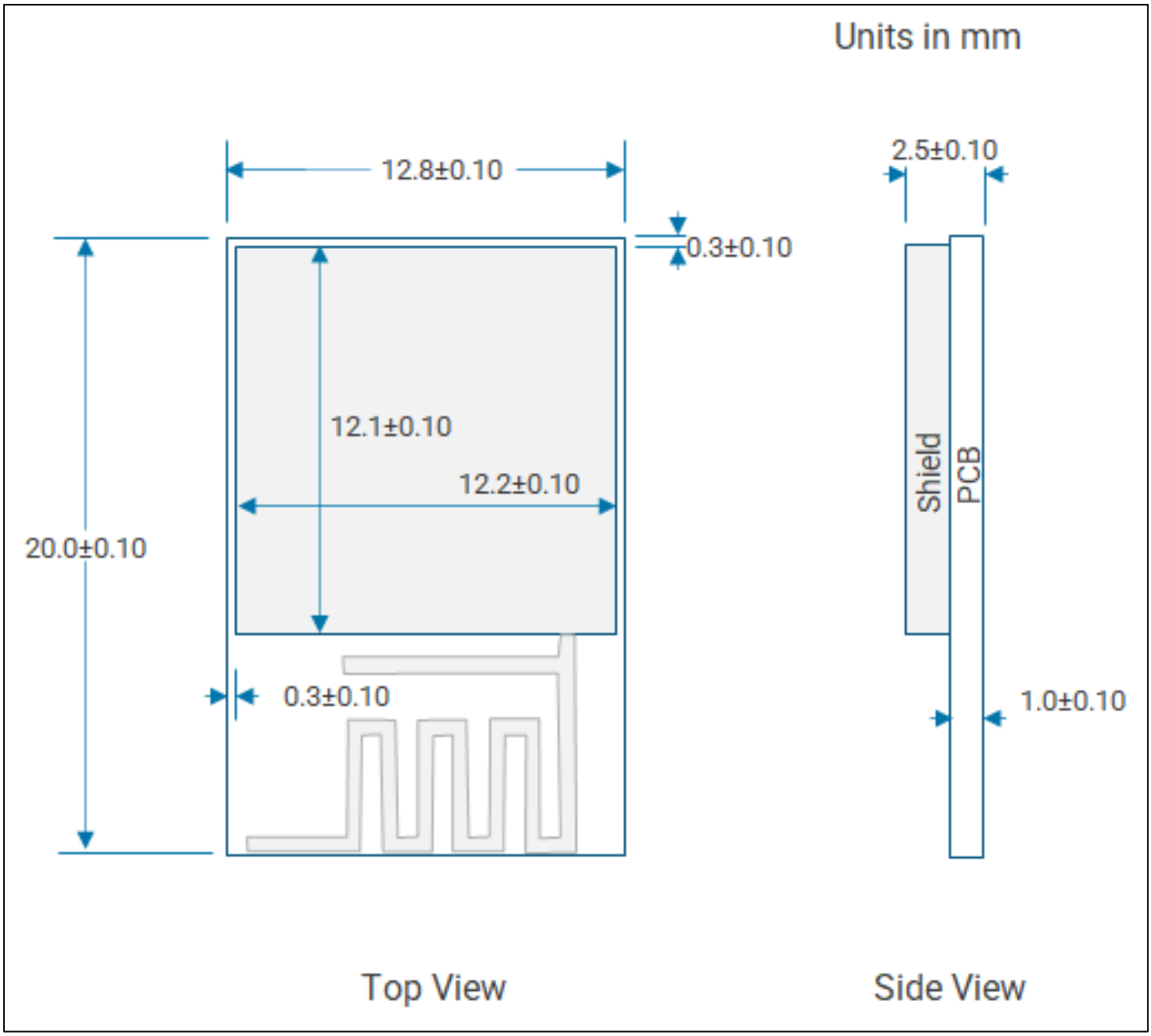


Figure 6: INP1014 module dimensions

INP1015

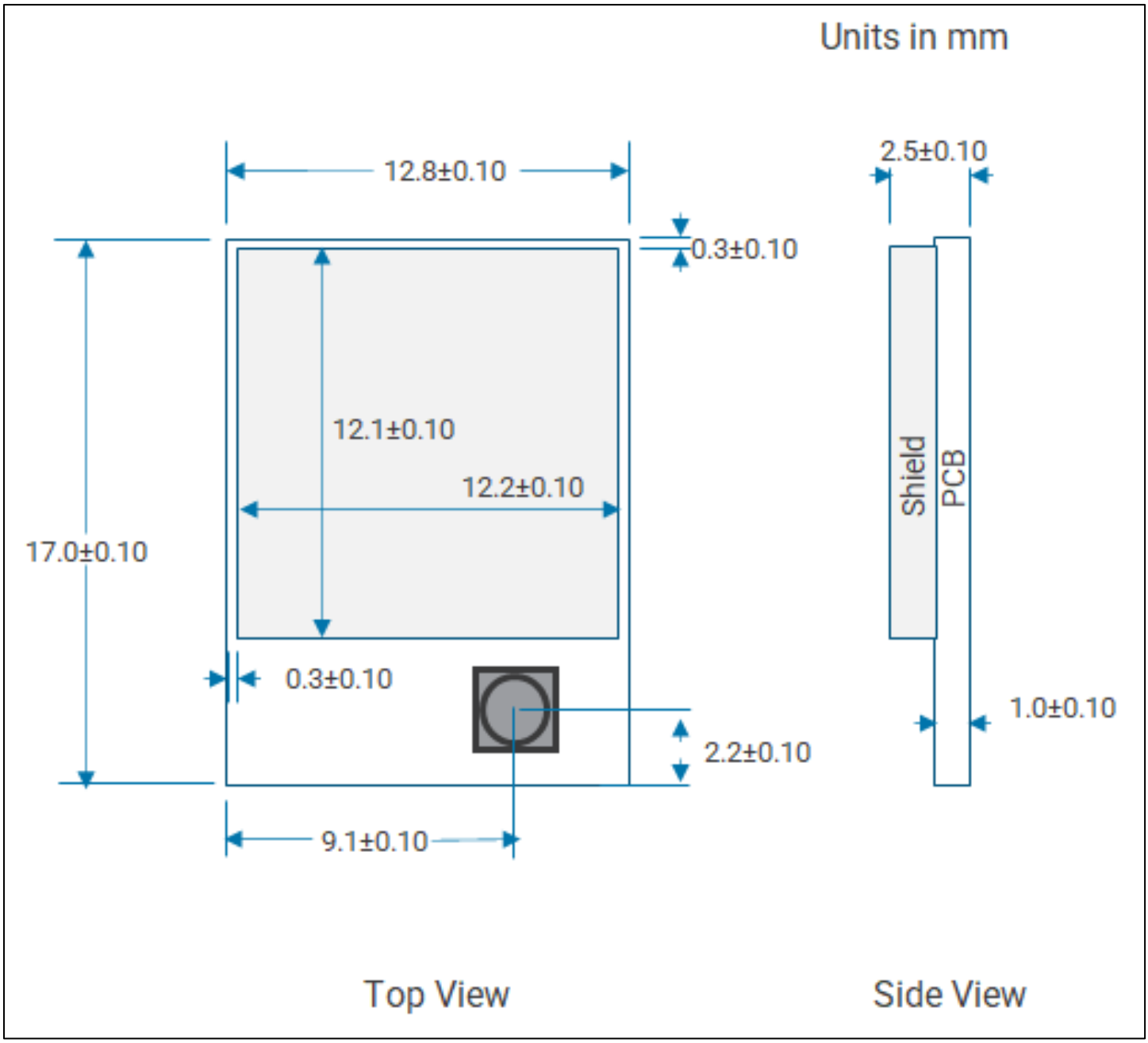


Figure 7: INP1015 module dimensions

Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
Storage Temperature		-40	+125	°C
Supply Voltages	V_3.3V	-0.3	4.0	V
RF Signal Input (INP1011 Module Only)		--	+10	dBm

Table 2: Absolute maximum ratings

Storage Conditions

Product is applicable to MSL3 based on JEDEC Standard J-STD-020. Product should be used within 12 months after receipt. If used after 12 months, the solderability should be confirmed. After the packing is opened, the product shall be stored at <30deg.C / <60%RH and the product shall be used within 168 hours, after this timeframe the product should be baked at 125°C for 24 hours. The products shall be baked on the heat-resistant tray as the shipment tray is not a heat-resistant, bakeable tray.

Operating Conditions

Parameter		Min.	Typical	Max.	Unit
Operating Temperature		-40	25	+85	°C
Input Supply Voltage Range	V_3.3V	--	3.6	V	
Input Supply Specification Voltage Range[1]	$V\_3.3V_{op}$	3.0		3.6	V
Input Supply Current (Tx Mode)	$I_{V\_3.3V}$	--	190	500	mA
VDDIO Voltage (Output)	VDDIO	2.5	--	3.0[2]	V
VDDIO Current (Supply)	$VDDIO_{Imax}$	--	--	20[3]	mA
Chip Enable[4]	EN_CHIP	--	3.3	--	V

Table 3: Operating conditions

Notes:

1. Recommended operational voltage range
2. Input Supply Voltage (V_3.3V) level must be ≥ 3.15V to achieve maximum 3.0V VDDIO voltage
3. 20mA max. (@ V_3.3V = 3.0V to 3.6V)
4. Chip enable must be held high for operating mode, either through external pullup resistor to V_3.3V or through GPIO connection to external device (For example: MCU or RTC)

Module Pin-outs

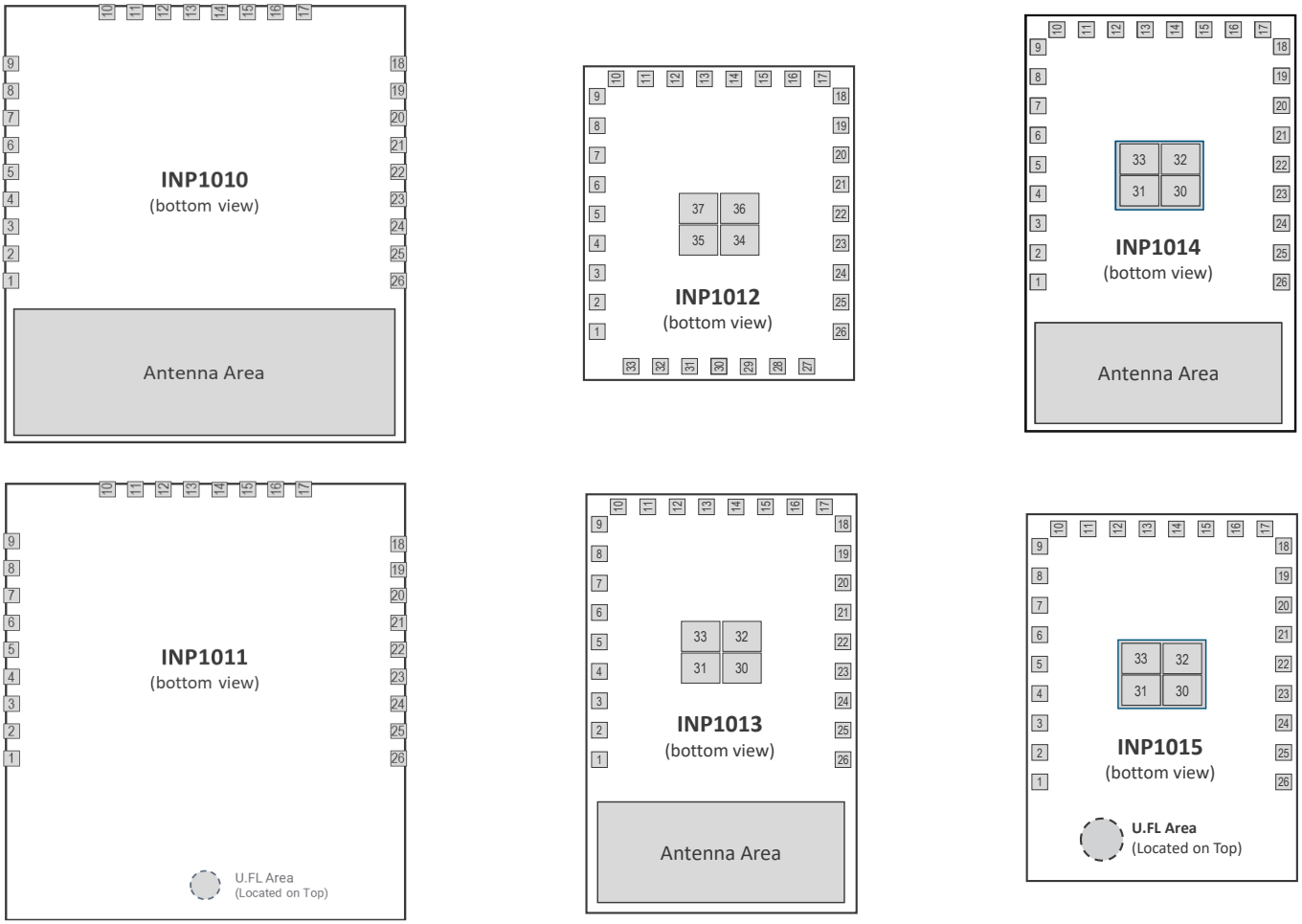


Figure 8: INP101x module pin-outs

Note: Module pin-out images are not to scale.

PIN TABLE	GND	GND (RF)	RFIO (Ant.)	V_3.3V	EN_CHIP	VDDIO	ADC_IN	GPIO14	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO17	GPIO18	GPIO19	GPIO20	GPIO21
INP1010	1,4,5,6,7,8,9,24,26	N/A	N/A	2,3	10	18	25	11	12	13	14	15	16	17	19	20	21	22	23
INP1011		N/A	N/A																
INP1012	1,4,5,6,7,8,9,24,26,34,35,36,37	27,28,29,31,32,33	30																
INP1013	1,4,5,6,7,8,9,24,26,30,31,32,33	N/A	N/A																
INP1014		N/A	N/A																
INP1015		N/A	N/A																

Table 4: INP101x module pin-out details

GPIO Specifications and Requirements

Digital I/O Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
Pull-Up Resistance (All GPIO except GPIO18)	R_{PU}	--	51	--	kΩ
Pull-Down Resistance (Only GPIO18, for JTAG TCK)	R_{PD}	--	51	--	kΩ
Pin Capacitance	C_{IN}		1.7		pF
V_3.3V = 3.3V, VDDIO = 2.5V, 25°C					
High Level Input Voltage	V_{IH}	2.0	--	3.6	V
Low Level Input Voltage	V_{IL}	-0.3	--	0.8	V
High Level Input Current	I_{IH}	--	2.0	--	nA
Low Level Input Current	I_{IL}	--	2.0	--	nA
High Level Output Voltage	V_{OH}	2.3	--	--	V
Low Level Output Voltage	V_{OL}	--	0.2	0.4	V
High Level Source Current	I_{OH}	--	8	--	mA
High Level Source Current, High Drive	I_{OH-HD}	--	10	--	mA
Low Level Sink Current	I_{OL}	--	7	--	mA
Low Level Source Current, High Drive	I_{OL-HD}	--	9	--	mA

Table 5: Digital I/O specifications

Peripheral Signal Mapping

Interface	Signal	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO14	GPIO17	GPIO18[4]	GPIO19[3]	GPIO20	GPIO21
UART	RXD			●									
	TXD		●										
	CTS												
	RTS												
Console	TX								●				
SPI Slave	CLK	●											
	CS						●						
	MOSI		●										
	MISO			●									
SDIO	SDIO_CLK												
	SDIO_CMD												
	SDIO_DATA0												
	SDIO_DATA1												
	SDIO_DATA2												
	SDIO_DATA3												
SPI Master (Software)	CLK												
	CS												
	MOSI												
	MISO												
GPIO[1]	GPIO												
PWM	PWM_0												
	PWM_1												
	PWM_2												
	PWM_3												
JTAG / SWD	TCK/ SWCLK									●			
	TMS / SWDIO										●		
	TDI											●	
	TDO / SWO												●
I2C	SCL												
	SDA												
I2S	SCK												
	WS												
	SD												

Table 6: Peripheral Signal Mapping

Legend:

● = Default Power-Up GPIO

■ = Function Supported on GPIO

■ = Required for factory production firmware loading in-situ. These should be connected to Host MCU or a header/connector to factory test/PC equipment. For UART with flow control also use GPIO0 and GPIO5. For higher speed factory programming the SPI connection is GPIO0, GPIO1, GPIO2, GPIO5

Notes:

1. Any GPIO can be used for wakeup (interrupt) and can drive high current loads such as LEDs.
2. IMPORTANT: All GPIO must be set to LOW during sleep mode for lowest power consumption.
3. IMPORTANT: Refrain from configuring GPIO19 as output LOW when power-save mode is enabled to ensure Talaria TWO operates as intended.
4. Only internal pull-down is available on GPIO18 (an external pull-up can be added, if required).

Peripheral Interface Specifications & Timing Diagrams

UART

The Talaria TWO modules include one (1) UART controller. All signals, RXD, TXD, CTS and RTS, can be individually programmed for use on any GPIO. The power-up default pin for TXD is GPIO1 and RXD is GPIO2.

UART Specification	Details
Maximum Baud Rate	921600
Minimum Baud Rate	300
Recommended Baud Rate	115200

Table 7: UART specifications

Console UART

Default pin is set to GPIO17, but it can be programmed to any GPIO. Unidirectional Tx only from Talaria TWO for debug purposes.

Console UART Specification	Details
Default Baud Rate	2457600

Table 8: Console UART specifications

SPI Slave

The Talaria TWO modules include one (1) SPI Slave interface. All signals are fixed to specific pins where CLK is GPIO0, MOSI is GPIO1, MISO is GPIO2 and CS is GPIO5. It is not possible to reassign the signals to different GPIOs.

SPI Slave Specification	Details
Maximum Clock Frequency	25MHz
Clock Polarity and Phase Modes Supported	Mode 0 (CPOL=0, CPHA=0) Mode 3 (CPOL=1, CPHA=1)
Data In/Out Sequence	MSB First
Other Features	Dual SPI Mode Capable Read Status Reset

Table 9: SPI Slave specifications

SPI Master (Software Implementation)

The Talaria TWO modules supports one (1) SPI Master interface via a software implementation. The four-wire implementation uses CLK, MOSI, MISO, and CS. It is possible to assign the signals to any GPIOs (except for GPIO18).

SPI Master Specification	Details
Maximum Clock Frequency	8MHz
Clock Polarity and Phase Modes Supported	Mode 0 (CPOL=0, CPHA=0) -OR- Mode 3 (CPOL=1, CPHA=1)
Data In/Out Sequence	MSB or LSB First

Table 10: SPI Master Specification

SDIO

The Talaria TWO modules support a standard 10MHz SDIO interface on GPIO0 through GPIO5.

SDIO Specification	Details
Maximum Clock Frequency	10MHz
SDIO Interface Specification	2.0

Table 11: SDIO Specification

I2C

The Talaria TWO modules include one (1) I2C bus interface that can serve as an I2C master or slave. The SCL and SDA lines can be individually programmed for use on any GPIO. Internal pull-up resistors are available for SCL/SDA on all GPIOs except for GPIO18 (GPIO18 only has internal pull-down resistors).

I2C Specification	Details
Data Rates	100Kbps, 400Kbps, 1Mbps
Address Modes	7-bit, 10-bit
Other Features	Send STOP at End NOSTART Before Msg IGNORE NAK From Slave

Table 12: I2C Specification

I2S

The Talaria TWO modules include one (1) I2S interface that can serve as an I2S master or slave. It is only capable of transmitting data – it cannot receive I2S data. The SCK, WS and SD lines can be individually programmed for use on any GPIO.

I2S Specification	Details
Audio Formats Support	Up to HD Audio, Dual Channel Stereo (2x 16-bit @ 48kHz)

Table 13: I2S Specification

PWM

The Talaria TWO modules include four (4) PWM timers that can be programmed on any GPIO.

PWM Specification	Details
Base Frequency	40MHz
Duty Rate Range	0% to 100%
Pulse Alignment	Left Aligned
Other	Audio Capable

Table 14: PWM Specification

JTAG/SWD

Compliant with ARM JTAG/SWD standards for debug purposes.

Analog to Digital Converter (ADC) Specifications

The Talaria TWO modules have a 12-bit (10-bit effective) SAR ADC for measuring the internal supply voltage and temperature levels in addition to measuring an external voltage level through a specified ADC port. The ADC has configuration settings for sampling rate and results averaging.

ADC Specification	Details	Unit
ADC Input Channels	VBAT, TEMP, EXT	--
Sampling Rates	5, 10, 20, 40	Msps
Results Averaging	2, 4, 8, 16	# of Samples
External Voltage Input Range	0 to 1.0	V
Additional Delay for ADC Ready after Wakeup	5	µs

Table 15: ADC Specification

Wi-Fi Features

Wi-Fi Features	Details
Wi-Fi Standards Supported	802.11 b/g/n (2.4GHz Single-Band, 20MHz)
Wi-Fi Modes	Station Mode
Operating Channels	1-13
Number of TCP/UDP Sockets	4-16[1]
Number of Concurrent SSL Connections	2-4[1]
Wi-Fi Security	WPA2, WPA3, WPA2 Enterprise (EAP-PSK, EAP-TLS)
Application Security	TLS1.2

Table 16: Wi-Fi Features

Note: Dependent on memory allocations/configurations.

BLE Features

BLE Features	Details
BLE Standard Supported	BLE5.0
BLE Modes	Central, Peripheral
BLE Advanced Features Supported	LE Coding (S2,S8)/FEC (Long-Range) 2Mbps PHY Extended Advertising
PHY Rates Supported	2Mbps, 1Mbps, 512kbps, 125kbps
Connection Roles	GAP Peripheral or Central
Generic Attribute Profile Roles	GATT Client or Server
Number of Concurrent Sessions	4/8[1]
Command Interface	HCI over SPI/UART
Security	AES-128CCM

Table 17: BLE Features

Note: Dependent on memory allocations/configurations.

Advanced Security Elements

Hardware Crypto Engines

Category	Details
Block Modes	Counter, GF, OFB, ECB, CBC-MAC, CBC-ENC, CBC-DEC, XEX
Block Cores (encryption)	AES (128/256), DES, TDES, SMS4, GF
Stream Cores (Hashing)	RC4, Michael, CRC32, SHA-1/256

Table 18: Hardware Crypto Engines

Additional Hardware Security Capabilities

Additional hardware security capabilities include:

1. DMA: Linear, Circular and Descriptor based transfer options
2. E-Fuse Disable JTAG
3. PUF/Secure Vault – Key/certificate, pass phrase, and application data storage, based on SoC Fingerprint

Software Security Features

Category	Details
uECC APIs	1. Supports ECDH and ECDSA 2. Key generation, sign and verify functions 3. Secure Boot and FOTA signed ELF
Cipher APIs	1. Wrapper to Cipher Hardware 2. Tight integration with DMA for effortless encryption/decryption
DMA APIs	1. Automatic encryption/decryption of data without CPU involvement 2. Comprehensive modes to support various application needs

Table 19: Software Security Features

DC & RF Characteristics

General DC Characteristics

Specification		Details	Unit
Wi-Fi Idle Connected PS-Polling (3.3V, 802.11b, 1Mbps, Clean RF Environment)	DTIM = 1	414	µA
	DTIM = 3	151	µA
	DTIM = 5	97	µA
	DTIM = 10	57	µA
Sleep Current[1]		19	µA
Hibernate Mode (EN_CHIP Low)[3]		< 1	µA
EN_CHIP/RST Reset Voltage[4]		0.6	V

Table 20: General DC Characteristics

Note:

1. RTC operating, memory retained, 3.3V supply, GPIO must be set to LOW.
2. SRAM memory is not retained, RTC is off.
3. EN_CHIP/RST must be held below 0.6V to reset device.

DC & RF Characteristics Wi-Fi 802.11b 2.4GHz

Specification	IEEE802.11b
Mode	DSSS / CCK
Channel Frequency	2412 - 2472MHz
Data Rates	1, 2, 5.5, 11Mbps

Conditions:

25C, V_3.3V = 3.3V, VDDIO = 2.5V

1Mbps unless stated otherwise

DC Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Tx Current (@ 17.5dBm)	--	178	--	mA
Rx Current	--	31	--	mA
Tx Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Output Power	15.0	--	--	dBm
Error Vector Magnitude (EVM)	-22.0	--	--	dB
Out-of-Band Spurious Emissions				
30MHz – 1.00GHz (RBW = 100kHz)	--	--	-41	dBm/MHz
1.0GHz – 12.75GHz (RBW = 1MHz)	--	--	-41	dBm/MHz
Rx Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Rx Input Level Sensitivity				
DSSS, 1Mbps	--	-96	--	dBm
Adjacent Channel Rejection				
DSSS, 1Mbps	35	--	--	dB

Table 21: DC & RF Characteristics Wi-Fi 802.11b 2.4GHz – 1Mbps

DC & RF Characteristics Wi-Fi 802.11g 2.4GHz

Specification	IEEE802.11g
Mode	OFDM
Channel Frequency	2412 - 2472MHz
Data Rates	6, 9, 12, 18, 24, 36, 48, 54Mbps

Conditions:

25C, V_3.3V = 3.3V, VDDIO = 2.5V

6Mbps unless stated otherwise

DC Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Tx Current (6Mbps @ 15.5dBm)	--	134	--	mA
Tx Current (54Mbps @ 15.5dBm)	--	100	--	mA
Rx Current (6Mbps)	--	34	--	mA
Rx Current (54Mbps)	--	35	--	mA
Tx Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Output Power (6 to 48Mbps)	15.5	--	--	dBm
Output Power (54Mbps)	14	--	--	dB
Error Vector Magnitude (EVM) (54Mbps)	-25	--	--	dB
Out-of-Band Spurious Emissions				
30MHz – 1.00GHz (RBW = 100kHz)	--	--	-41	dBm/MHz
1.0GHz – 12.75GHz (RBW = 1MHz)	--	--	-41	dBm/MHz
Rx Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Rx Input Level Sensitivity				
OFDM, 6Mbps	--	-93	--	dBm
Adjacent Channel Rejection				
OFDM, 54Mbps	-1	--	--	dB

Table 22: DC & RF Characteristics Wi-Fi 802.11g 2.4GHz – 1Mbps

DC & RF Characteristics Wi-Fi 802.11n 2.4GHz

Specification	IEEE802.11n
Mode	OFDM
Channel Frequency	2412 - 2472MHz
Data Rates	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps

Conditions:

25C, V_3.3V = 3.3V, VDDIO = 2.5V

6.5Mbps (MCS0) unless stated otherwise

DC Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Tx Current (MCS0 @12.5dBm)	--	108	--	mA
Tx Current (MCS7 @ 12.5dBm)	--	81	--	mA
Rx Current (MCS0)	--	34	--	mA
RX Current (MCS7)	--	37	--	mA
Tx Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Output Power (MCS 0-4)	15.5	--	--	dBm
Output Power (MCS 5)	15	--	--	dB
Output Power (MCS 6)	10	--	--	dB
Output Power (MCS 7)	4	--	--	dB
Error Vector Magnitude (EVM) (MCS 7)	-27.0	--	--	dB
Out-of-Band Spurious Emissions				
30MHz – 1.00GHz (RBW = 100kHz)	--	--	-41	dBm/MHz
1.0GHz – 12.75GHz (RBW = 1MHz)	--	--	-41	dBm/MHz
Rx Characteristics	**Min.**	**Typical**	**Max.**	**Unit**
Rx Input Level Sensitivity				
OFDM, 6.5Mbps	--	-92	--	dBm
OFDM, 65Mbps	--	-69	--	dBm

Adjacent Channel Rejection				
OFDM, 54Mbps	TBD	--	--	dB

Table 23: DC & RF Characteristics Wi-Fi 802.11n 2.4GHz – 1Mbps

DC & RF Characteristics BLE

Specification (3.3V)	Typical	Unit
BLE Receive Current @ 2Mb/s	30	mA
BLE Receive Current @ 1Mb/s	29	mA
BLE Receive Current @ 500Kb/s	30	mA
BLE Receive Current @ 125Kb/s	31	mA
BLE Transmit Current @ 0dBm 2Mb/s	27	mA
BLE Transmit Current @ 0dBm 1Mb/s	26	mA
BLE Transmit Current @ 0dBm 500Kb/s	39	mA
BLE Transmit Current @ 0dBm 125Kb/s	53	mA
BLE Transmit Current @ 10dBm 2Mb/s	38	mA
BLE Transmit Current @ 10dBm 1Mb/s	36	mA
BLE Transmit Current @ 10dBm 500Kb/s	59	mA
BLE Transmit Current @ 10dBm 125Kb/s	81	mA
BLE Advertising (300ms Interval, 3-Channels)	330	µA
BLE Advertising (300ms Interval, 2-Channels)	280	µA
BLE Advertising (300ms Interval, 1-Channel)	190	µA
Maximum Conducted BLE Power Out (FCC)	9.1	dBm
Maximum Conducted BLE Power Out (ETSI)	6.0	dBm

Table 24: DC & RF Characteristics BLE

Technology	Test Case	Measurement	Data Rate	Set Tx Pout (dbm)	Average	Unit
BLE Tx	In-Band ACP Emission	ACP_±2	2LE	0	-33.45	dBm
			1LE	0	-47.04	
			500KLE	0	-46.67	
			125KLE	0	-46.86	
		ACP_±3	2LE	0	-52.81	dBm
			1LE	0	-56.12	
			500KLE	0	-55.83	
			125KLE	0	-55.84	
		ACP_±>3	2LE	0	-58.49	dBm
			1LE	0	-52.83	
			500KLE	0	-51.96	
			125KLE	0	-52.64	
	Modulation Characterization	Δf1	2LE	0	500.18	kHz
			1LE	0	250.41	
		Δf2	2LE	0	436.27	
			1LE	0	226.82	
		Δf2/f1	2LE	0	0.87	
			1LE	0	0.91	
BLE Rx	Rx Sensitivity	Sens	2LE	N/A	-89.21	dBm
			1LE	N/A	-91.45	
			500KLE	N/A	-97.49	
			125KLE	N/A	-100.15	

Table 25: Technology with test case details

Power Schemes

Power-Up Timing Diagrams

Specification	Symbol	Min.	Typ.	Max.	Unit
V_3.3V Supply Rise Time from 10% to 90%	T_r	40	--	80	µs
Power ON to EN_CHIP Release	T_{EN}	100	--	--	µs
Power ON to VDDIO Ready	T_{IO}	--	--		µs
Power ON to CPU Ready	T_{pu}	--	--	630	µs

Table 26: Power-up timings diagrams

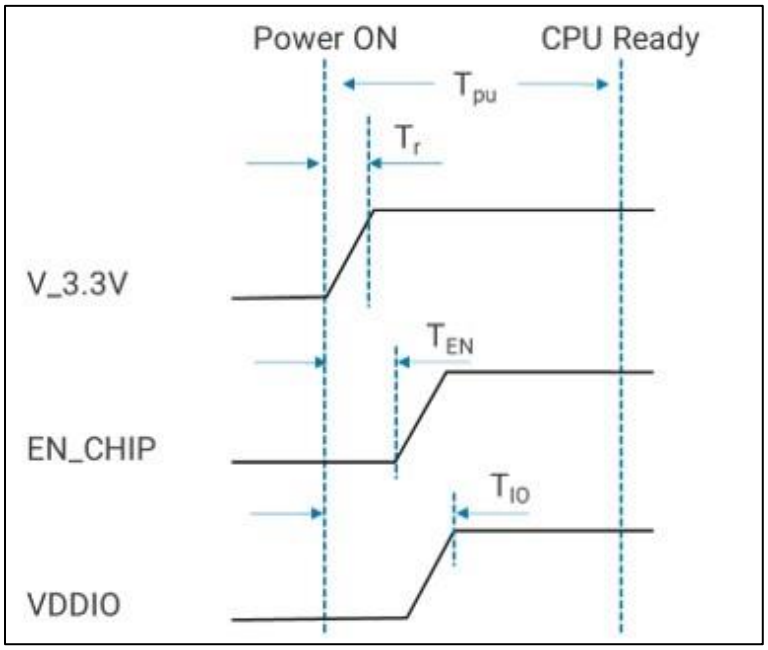


Figure 9: Power-up

Note:

1. All GPIOs must be low or undriven on Power-Up.
2. EN_CHIP must be held low until after TEN.
3. VDDIO must be low or undriven on Power-Up.

Wakeup Timing Detail

1. Wakeup from Sleep on Internal Timer
    a. Wakeup to CPU Ready – 550us
    b. Wakeup to Transmit/Receive (Tx/Rx) – 1ms
2. Wakeup from Sleep using GPIO Wakeup Pin / UART Rx
    a. Wakeup to CPU Ready – 550us

Reset Timing Diagrams

Specification	Symbol	Min.	Typ.	Max.	Unit
Reset Duration	T_{EN}		165		ms

Table 27: Reset timing specifications

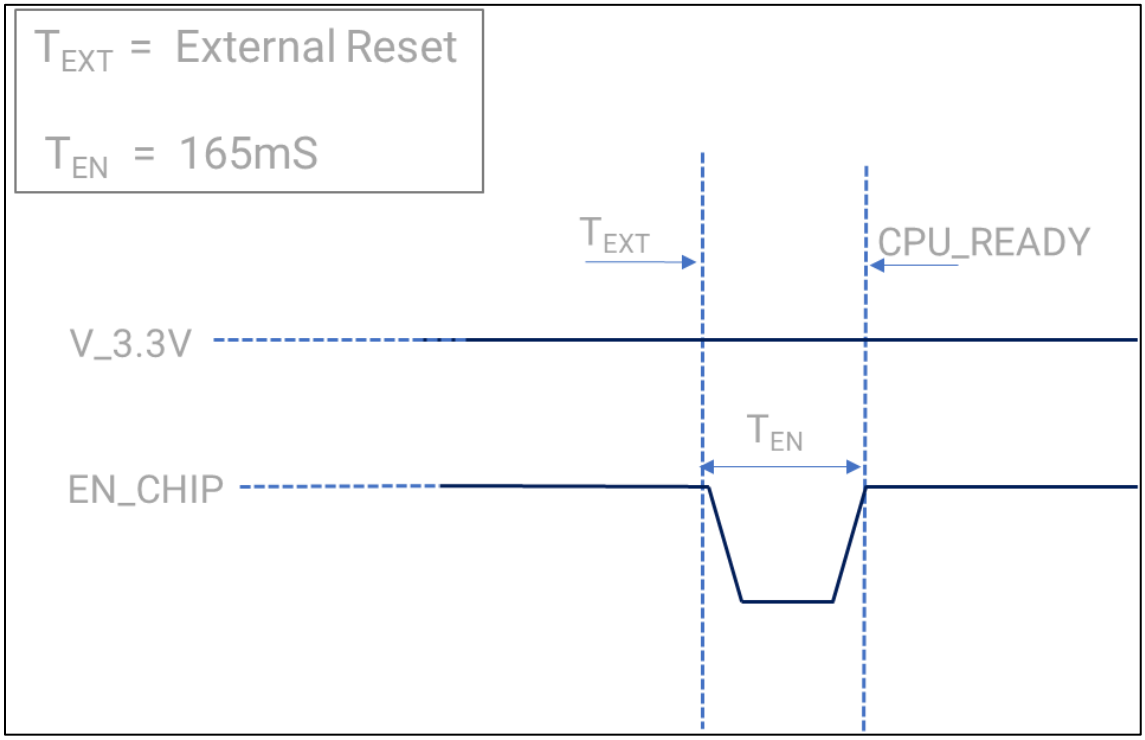


Figure 10: Reset Timing Diagram

Module Schematics

INP1010 Module Schematics

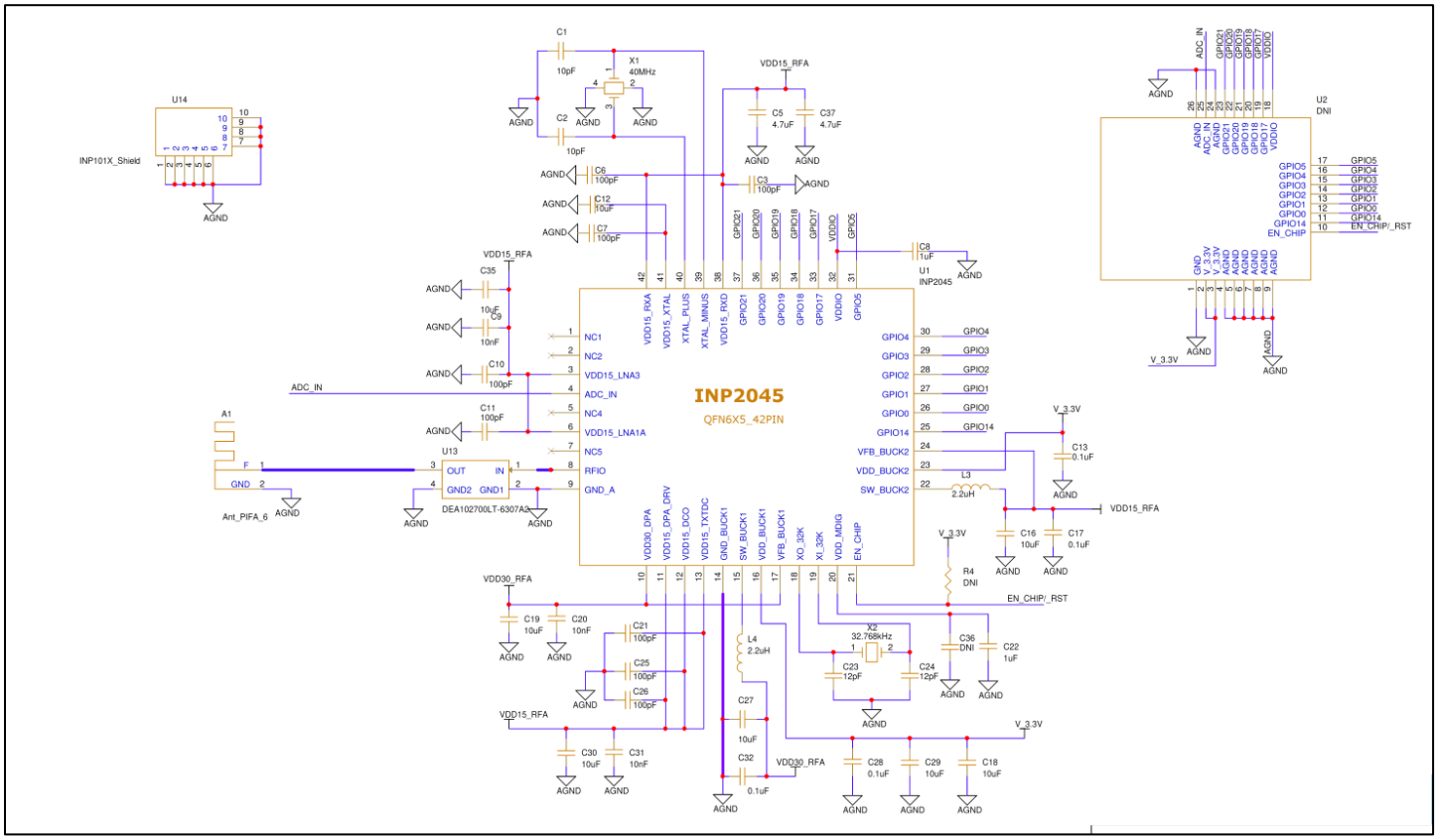


Figure 11: INP1010 Module Schematics

INP1011 Module Schematics

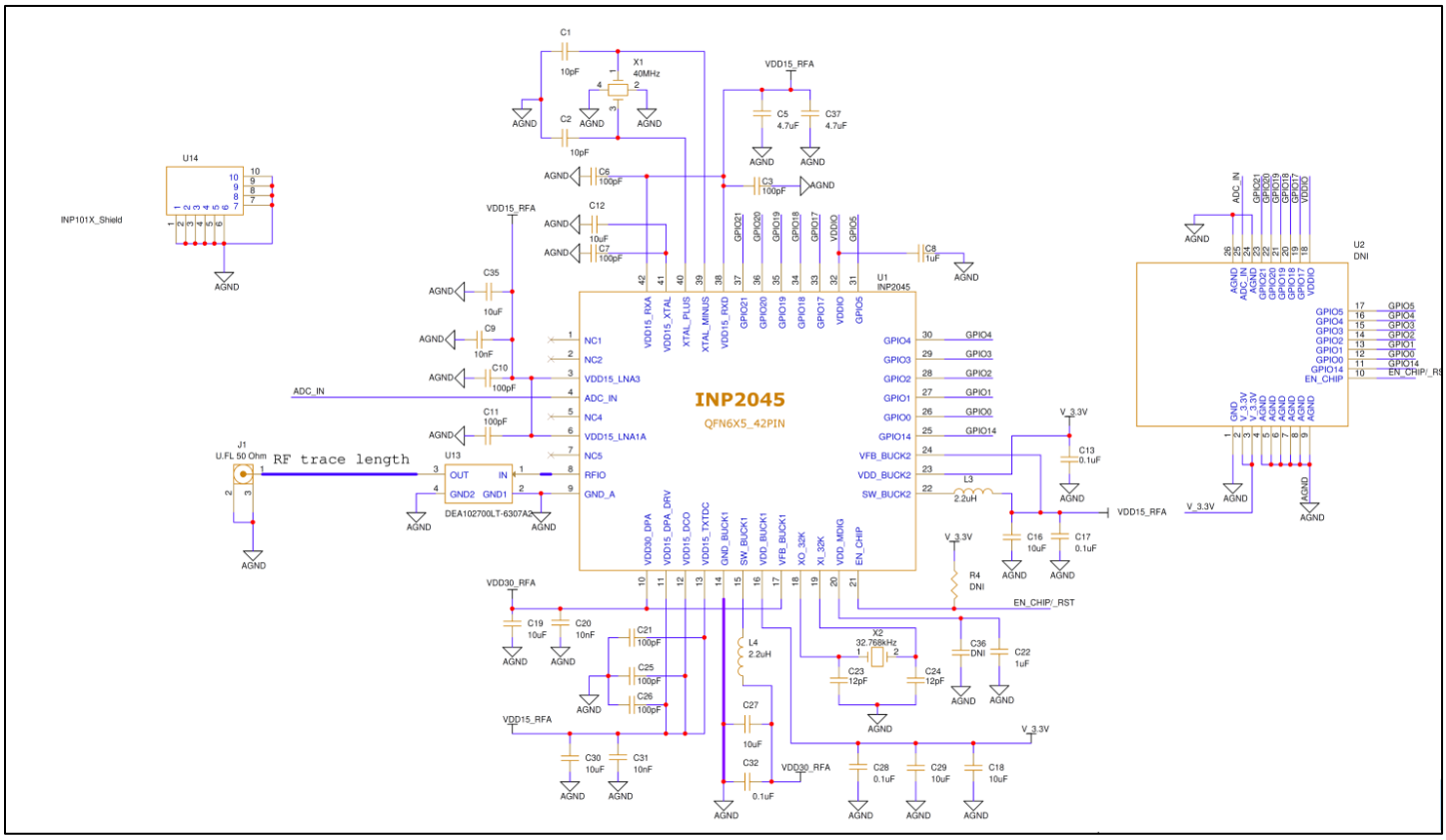


Figure 12: INP1011 Module Schematics

INP1012 Module Schematics

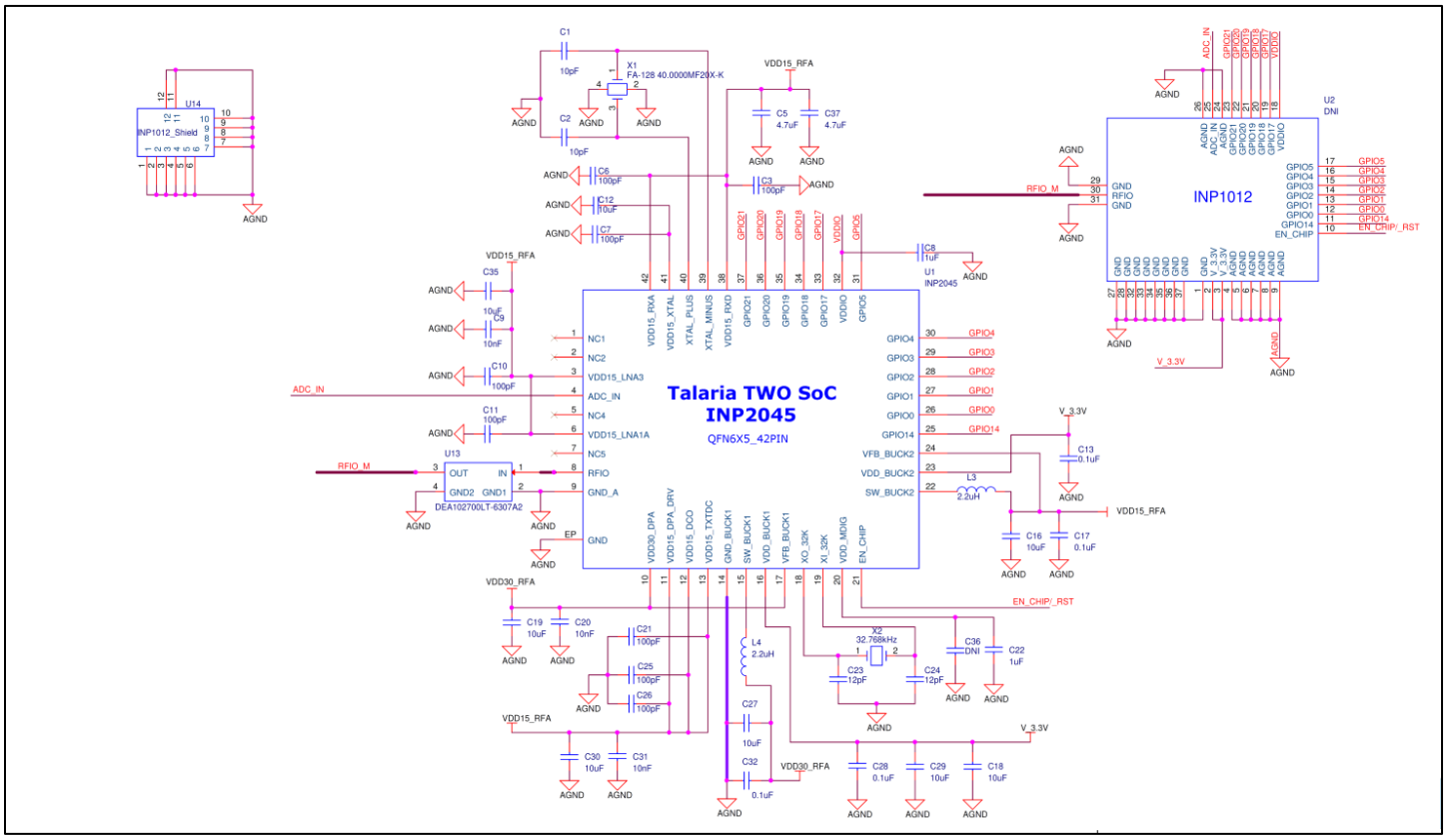


Figure 13: INP1012 Module Schematics

INP1013 Module Schematics

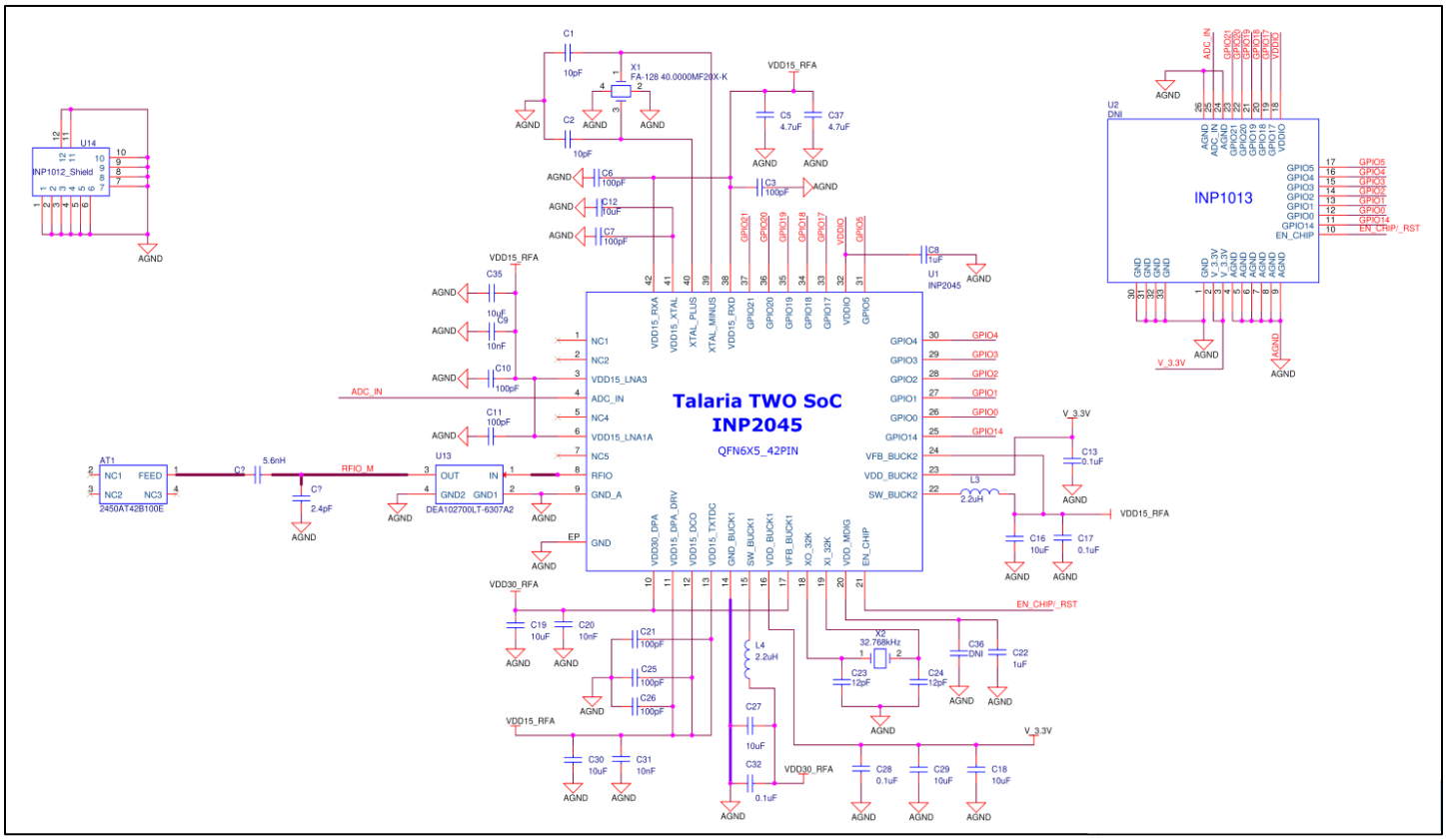


Figure 14: INP1013 Module Schematics

INP1014 Module Schematics

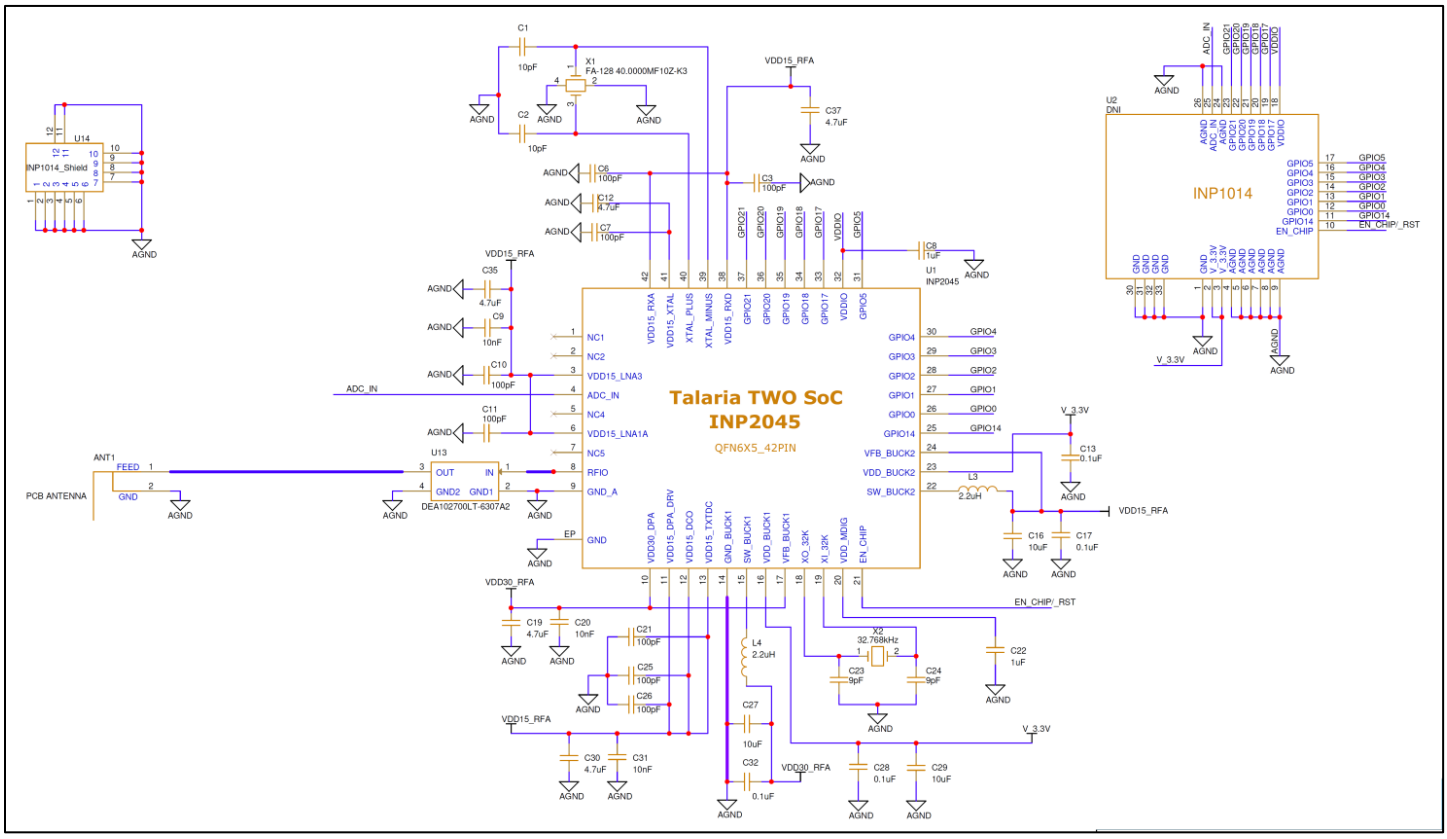


Figure 15: INP1014 Module Schematics

INP1015 Module Schematics

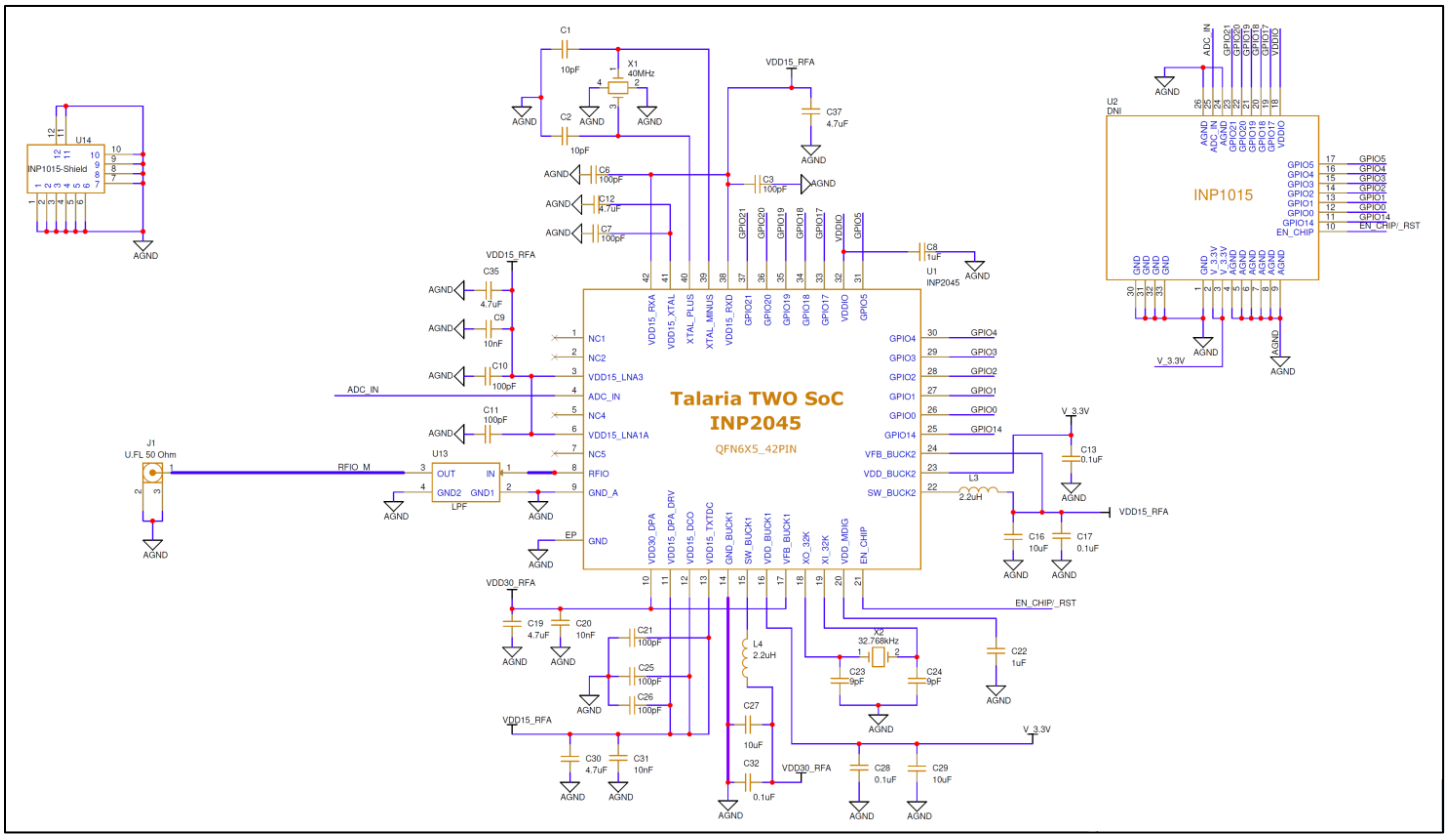


Figure 16: INP1015 Module Schematics

Recommended PCB Landing Pad Pattern

INP1010 and INP1011 Landing Pad Pattern

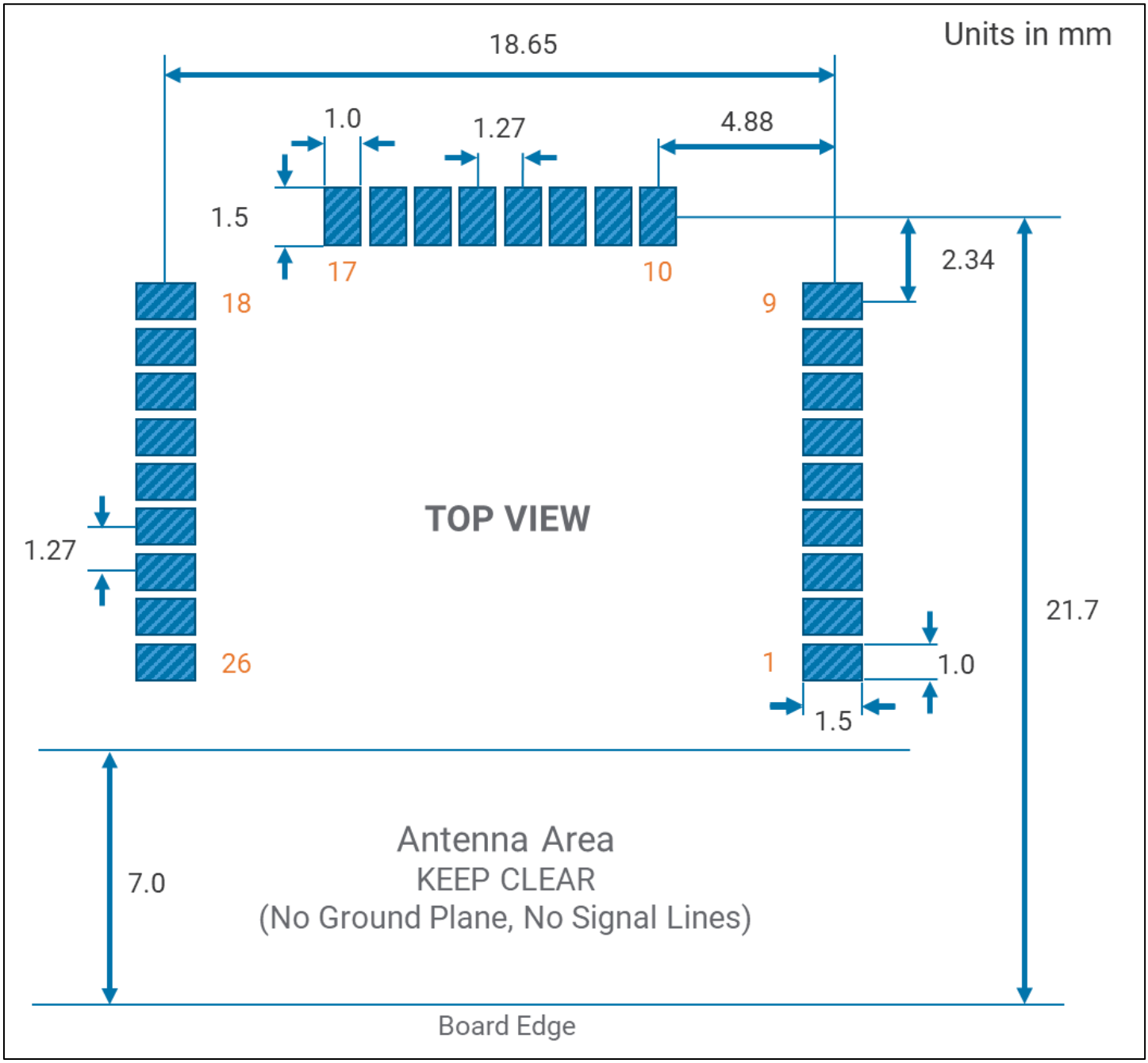


Figure 17: PCB Landing Pad Pattern - INP1010/11

INP1012 Landing Pad Pattern

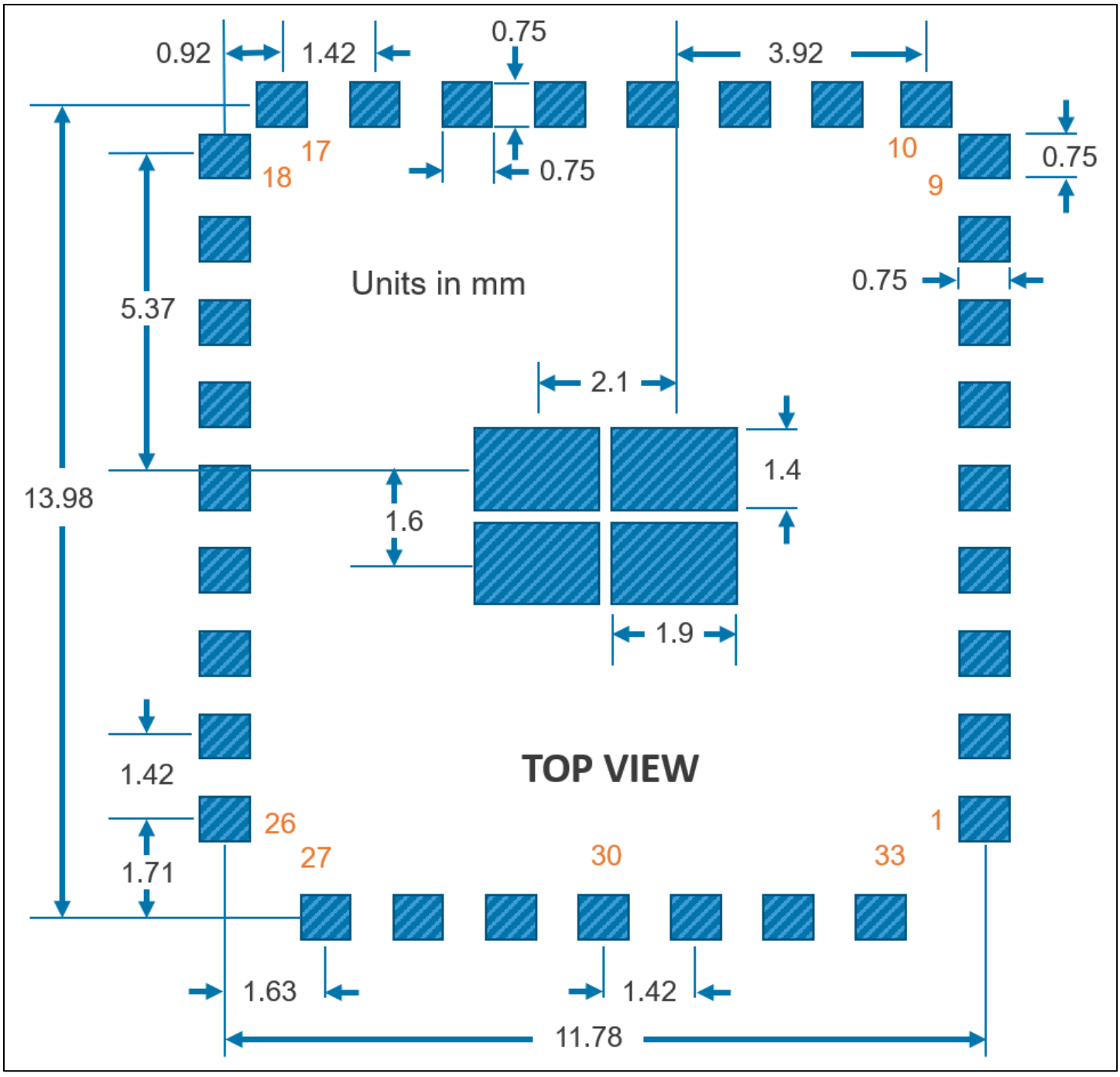


Figure 18: PCB Landing Pad Pattern - INP1012

INP1013 / INP1014 / INP1015 Landing Pad Pattern

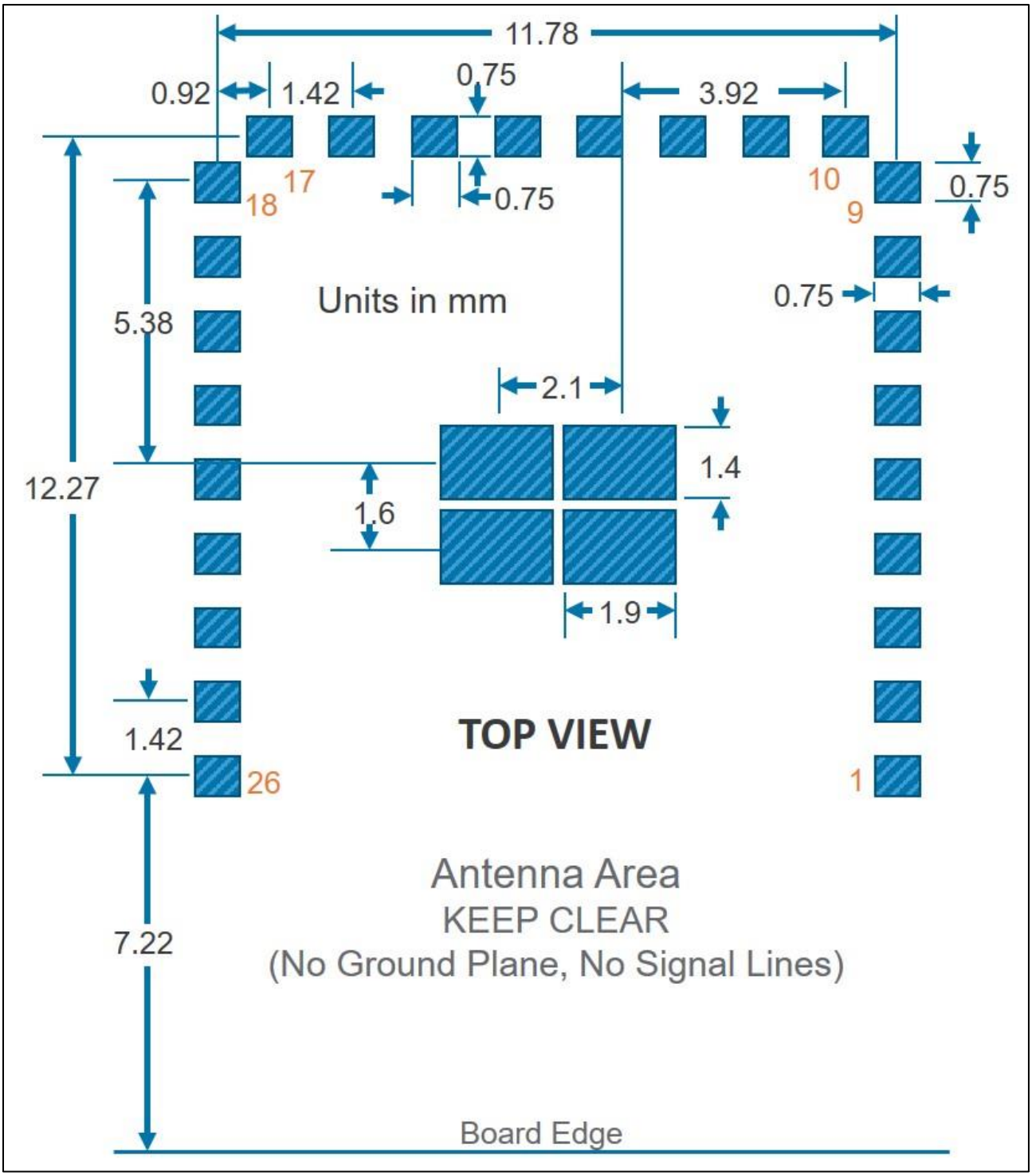


Figure 19: PCB Landing Pad Pattern - INP1013

Recommended Reflow Profile

Recommend Reflow Profile based on IPC/JEDEC J-STD 020:

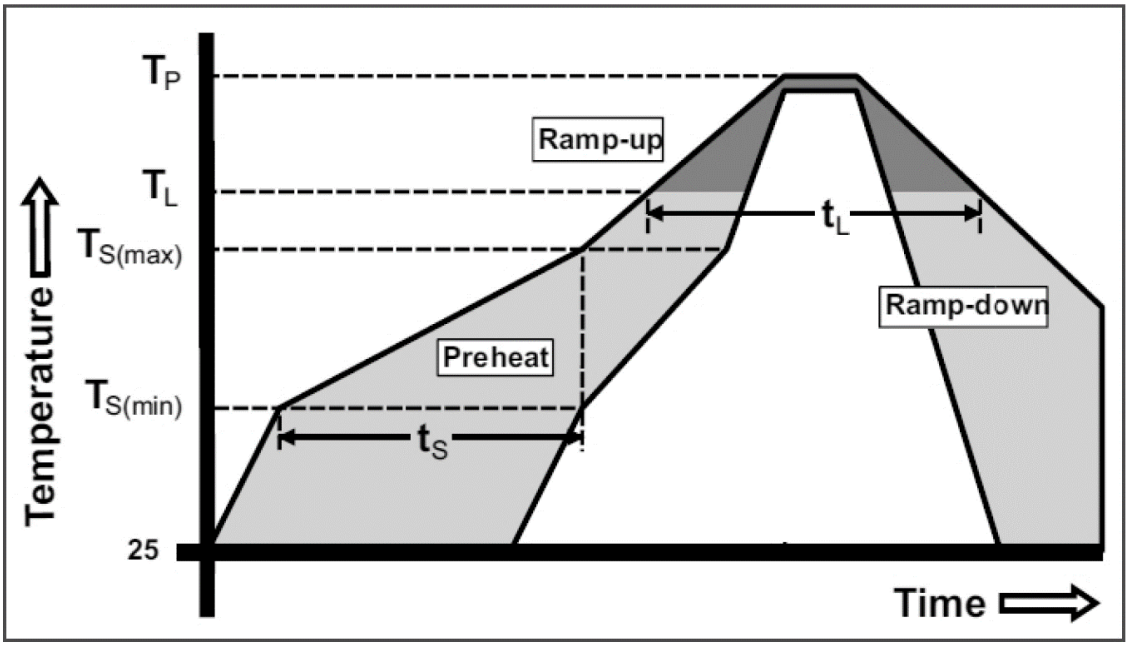


Figure 20: Recommended Reflow Profile

Reflow Condition	IPC/JEDEC J-STD 020	Pb-Free Assembly
Pre-Heat / Soak	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (t_S) from $T_{S(min)}$ to $T_{S(max)}$)	60 to 120 seconds
Ramp-up Rate from T_L to T_P		3°C/second max.
Reflow	Liquidous Temperature (T_L)	217°C
	Time (t_L) to maintain above T_L	60 to 150 seconds
Peak package body temperature (T_P)		245°C
Ramp-down rate (T_P to T_L)		6°C/second max.

Table 28: Recommended Reflow Condition

RoHS and REACH Compliance

This module meets the requirements set forth by the RoHS and REACH directives.

Further details are available with InnoPhase Sales. Contact: sales@innophaseiot.com.

Packing Details

INP1010 and INP1011 Packing

ESD foam tray used for shipping (units in mm):

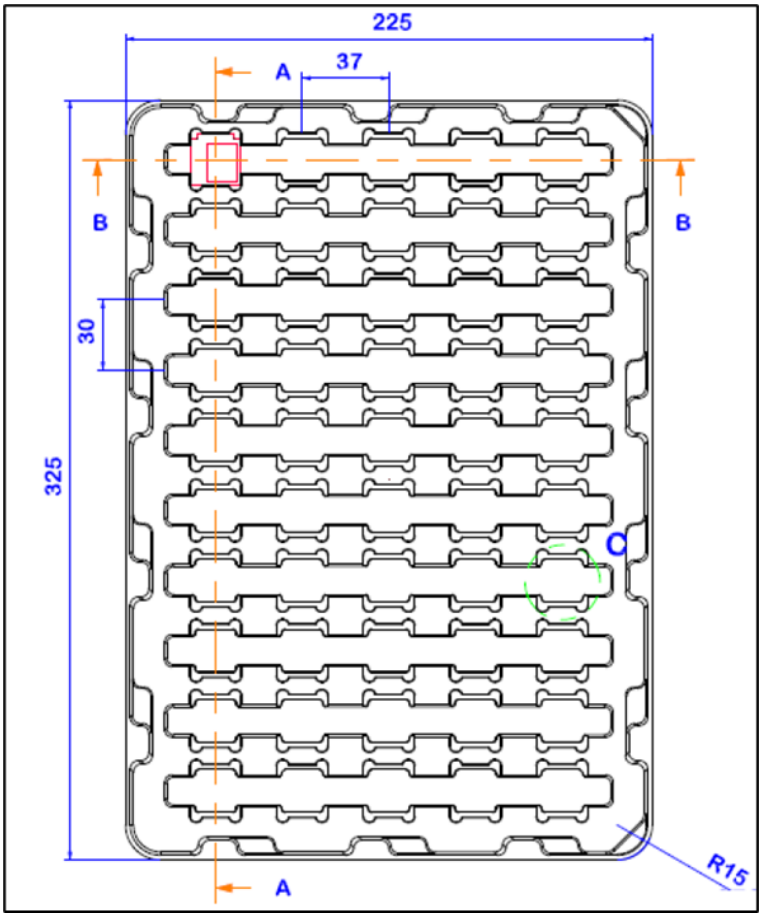
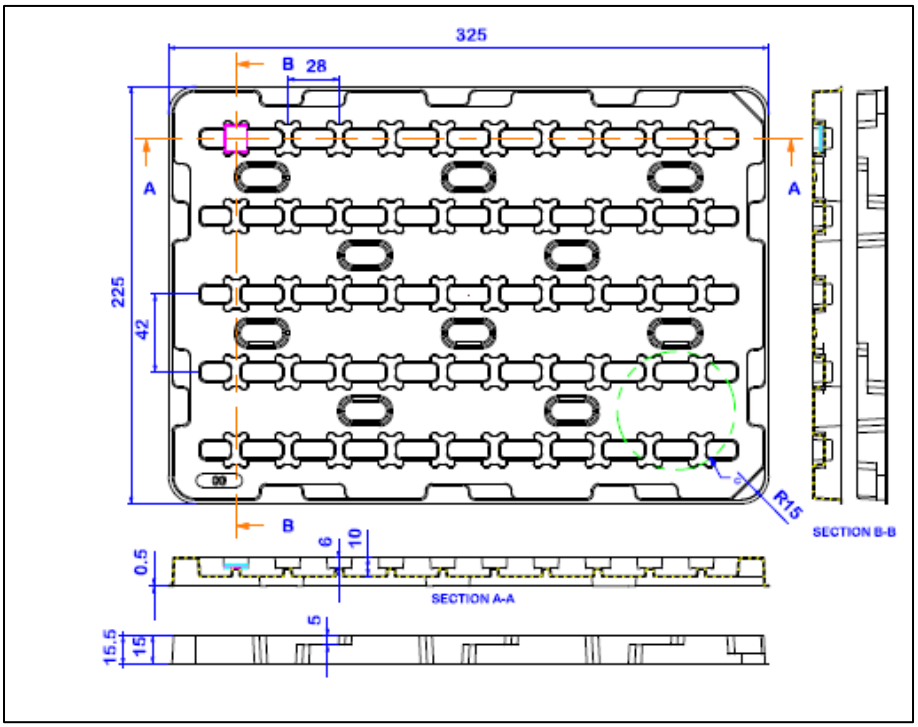


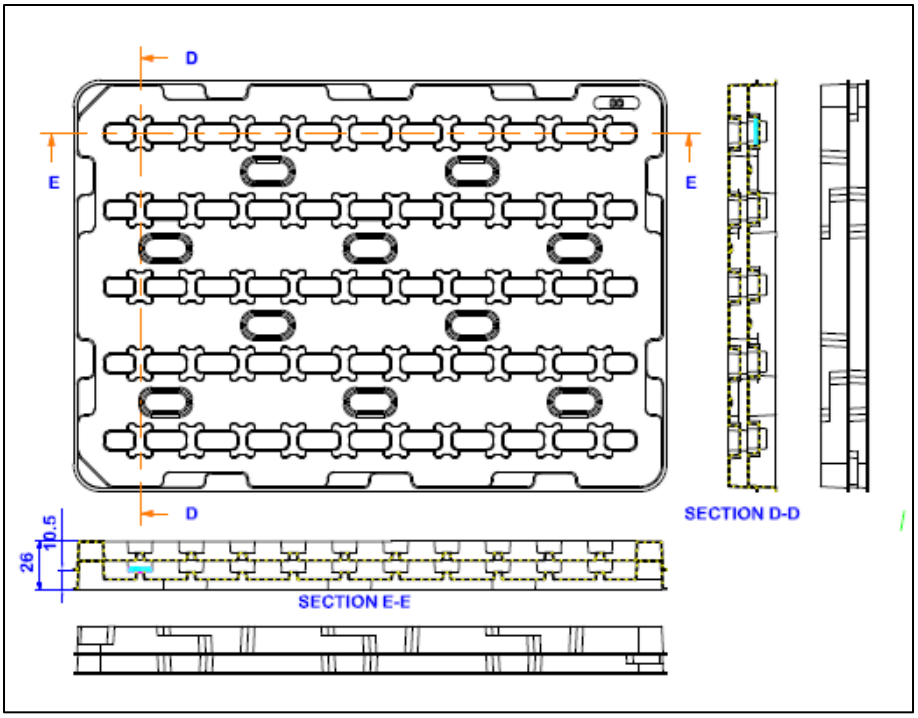
Figure 21: INP1010 and INP1011 Packing

Packing Details:
1 Tray = 50 Units
1 Inner Box = 10 Trays + 1 Empty Tray
1 Outer Box = 4 Inner Boxes

Table 29: INP1010/11 - Packing details

INP1012 Packing





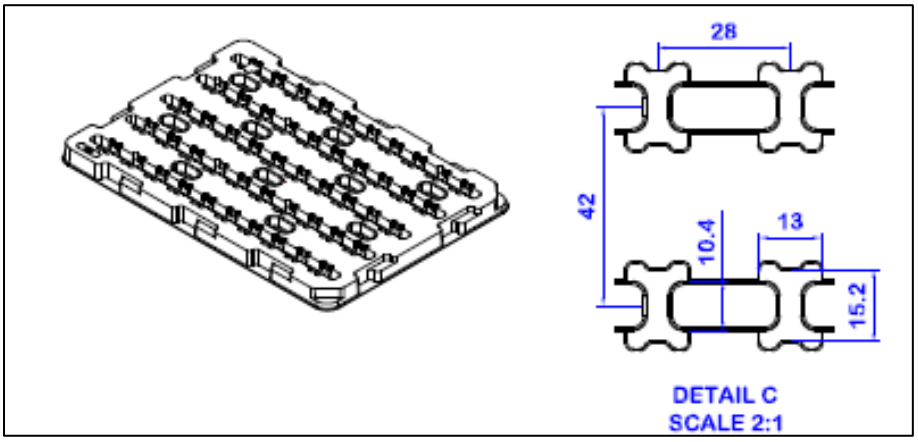
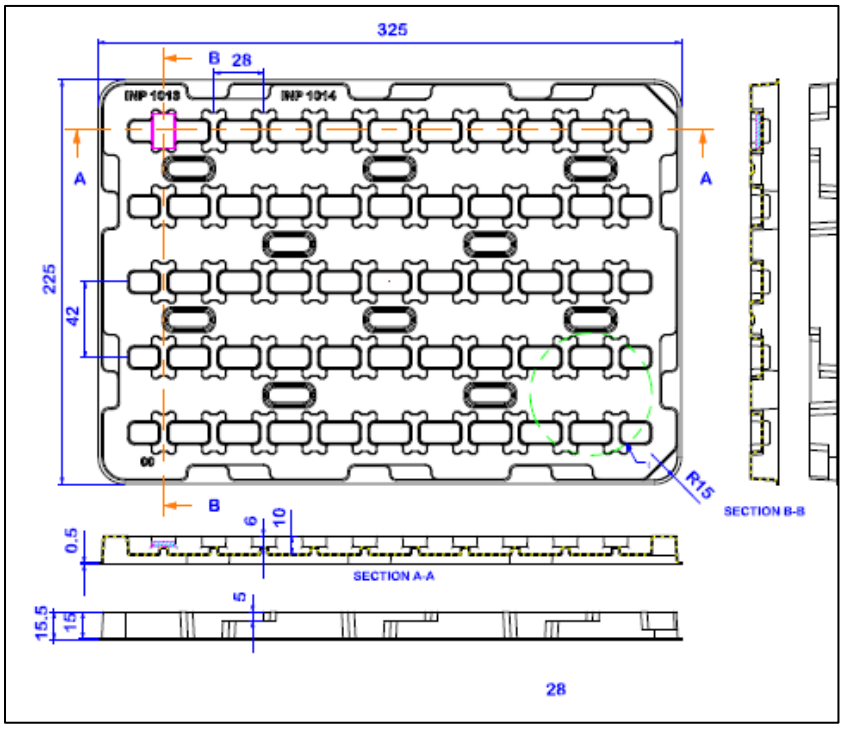


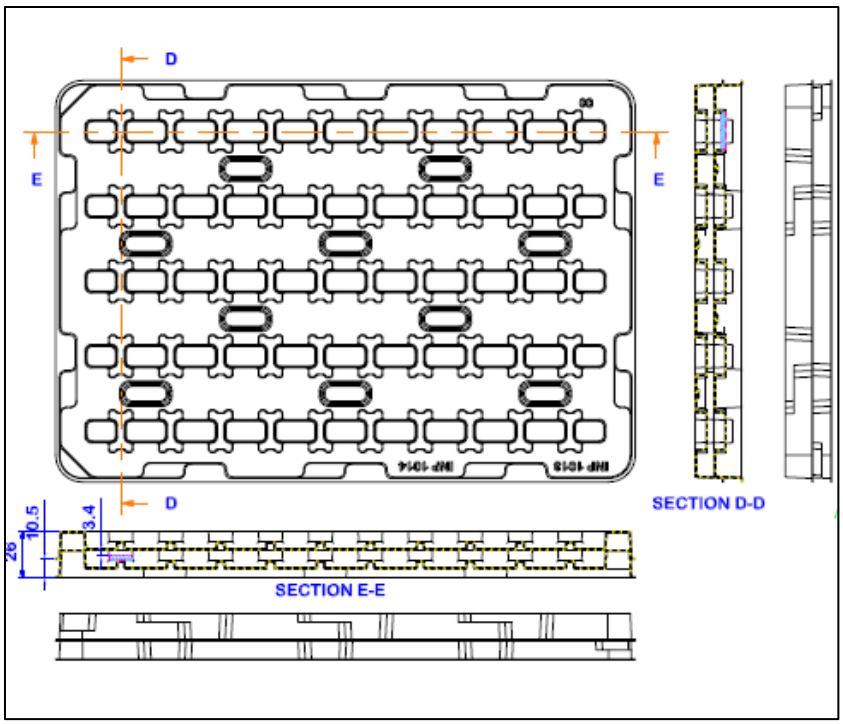
Figure 22: INP1012 - Packing details

Note:

1. Material: PS White Anti Coating
2. Thickness: 0.5mm
3. Tray are packed in plastic bag to prevent dirt and contamination
4. Thermal forming process with no mold release agent
5. Total 50 pocket/tray

INP1013 and INP1014 Packing





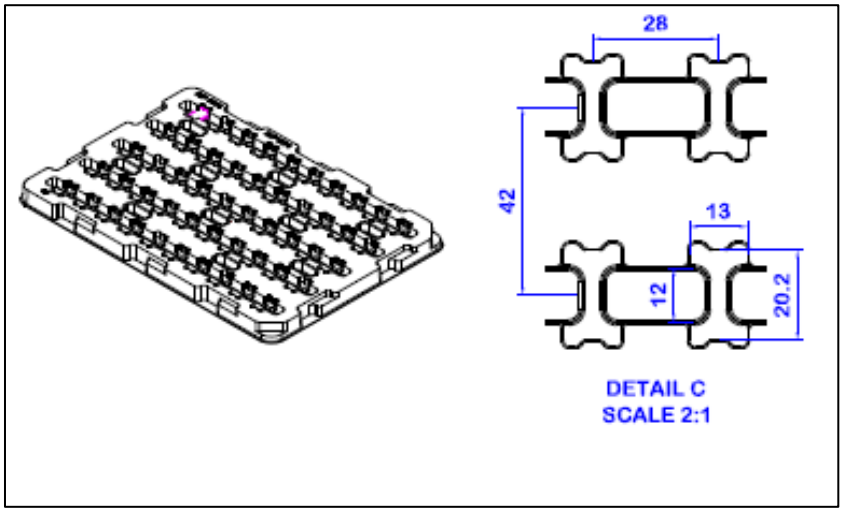


Figure 23: INP1013/14 - Packing details

Note:

1. Material: PS White Anti Coating
2. Thickness: 0.5mm
3. Tray are packed in plastic bag to prevent dirt and contamination
4. Thermal forming process with no mold release agent
5. Total 50 pocket/tray

INP2045 SoC Part Number

Manufacturer Part Number	Ordering Part Number	Package Type	Size	Shipment Method
INP2045	INP2045-H1-IRP	QFN-42	5 x 6 x 0.85mm 0.4 mm pitch	Tape & Reel 4Ku/Reel

Table 30: INP2045 SoC Part Number

INP2045 SoC Block Diagram

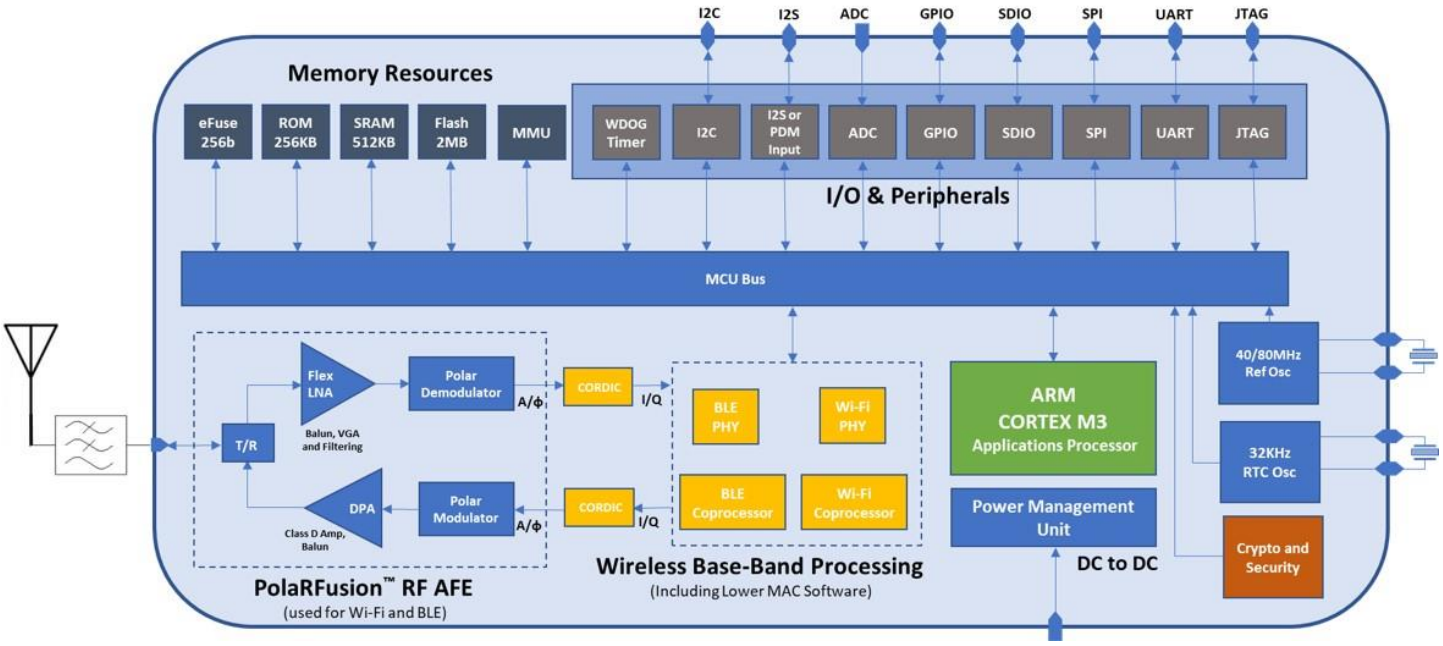


Figure 24: INP2045 SoC Block Diagram

INP2045 SoC Chip Pin Out and Dimensions

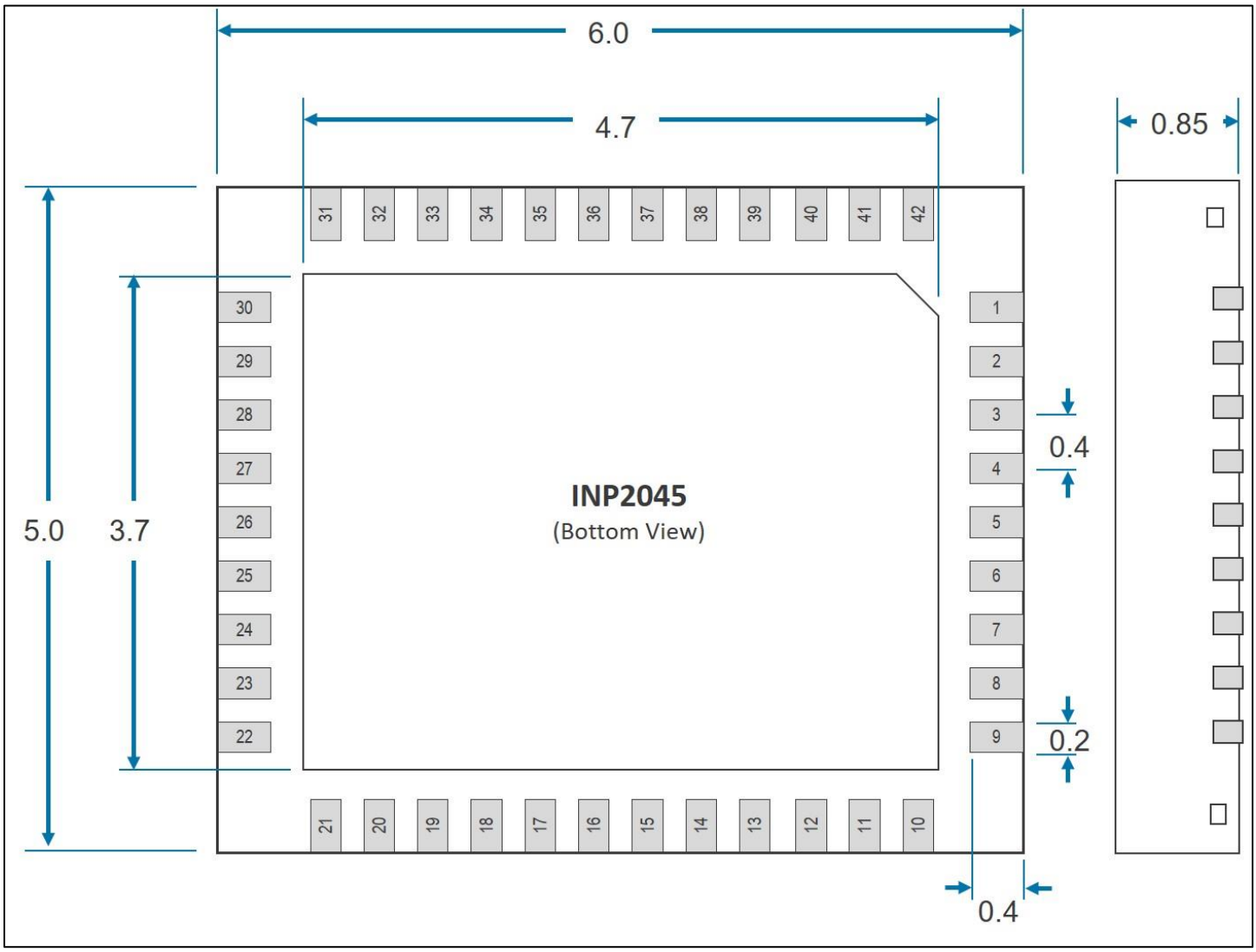


Figure 25: INP2045 SoC Chip Pin Out and Dimensions

INP2045 SoC Pin Description

PIN#	Type	Description
1	NC	No Connection
2	NC	No Connection
3	Power/Bypass	Local power bypass. Connect to Pin 24.
4	ADC_IN	ADC Analog Input (voltage range is 0-1 V)
5	NC	No Connection
6	Power/Bypass	Local power bypass. Connect to Pin 24.
7	NC	No Connection
8	RF	50-ohm Antenna RF Interface
9	Ground	Ground
10	Power/Bypass	Local power bypass. Connect to Pin 17.
11	Power/Bypass	Local power bypass. Connect to Pin 24.
12	Power/Bypass	Local power bypass. Connect to Pin 24.
13	Power/Bypass	Local power bypass. Connect to Pin 24.
14	Ground	Ground
15	Power	Connect 2.2µH inductor to Pin 17.
16	Power/Bypass	Main power (VDD) input and bypass. Connect to Pin 23.
17	Power/Bypass	Local power bypass.
18	XTAL	Connect to 32kHz crystal
19	XTAL	Connect to 32kHz crystal
20	Power/Bypass	Local power bypass.
21	Input	EN_CHIP (Chip enable), requires external pullup
22	Power	Connect 2.2µH inductor to Pin 24.
23	Power/Bypass	Main power (VDD) input and bypass. Connect to Pin 16.
24	Power/Bypass	Local power bypass.
25	I/O	GPIO pin, GPIO14
26	I/O	GPIO pin, GPIO0
27	I/O	GPIO pin, GPIO1
28	I/O	GPIO pin, GPIO2
29	I/O	GPIO pin, GPIO3
30	I/O	GPIO pin, GPIO4
31	I/O	GPIO pin, GPIO5

32	Power/Bypass	Local power bypass.
33	I/O	GPIO pin, GPIO17, Tx Console
34	I/O	GPIO pin, GPIO18
35	I/O	GPIO pin, GPIO19
36	I/O	GPIO pin, GPIO20
37	I/O	GPIO pin, GPIO21
38	Power/Bypass	Local power bypass. Connect to Pin 24.
39	XTAL	Connect to 40MHz crystal
40	XTAL	Connect to 40MHz crystal
41	Power/Bypass	Local power bypass.
42	Power/Bypass	Local power bypass. Connect to Pin 24.
43	Power/Bypass	Ground (Paddle)

Table 31: INP2045 SoC Pin Description

INP2045 SoC Electrical

Clocks and Timers

1. 40MHz crystal oscillator (external crystal)
2. 32KHz crystal oscillator (external crystal)
3. Internal 32KHz RC oscillator with calibration
4. 16 hardware timers /3 timebases
5. Watchdog timer

The InnoPhase INP2045 requires two external crystals (40MHz and 32kHz) which with internal circuitry create high precision internal clocks. The 40MHz clock is the reference for the high-speed system clocks including the CPU, co-processor, digital functions and the radio. The 32kHz clock is the timing source for low-frequency subsystems including power management, sleep timekeeping and some low-frequency logic. The INP2045 also provides an internal 32kHz oscillator which, in some applications, can be calibrated for sleep timekeeping needs without the need for the external 32kHz crystal.

The 40MHz crystal must meet ±10 ppm tolerance for best performance.

The 40MHz clock is disabled by the system during normal sleep operations to minimize power consumption. The 32kHz clock is continuously enabled when supporting fast wake-up features. The 32kHz clock and associated circuitry have been designed to operate at very low currents to provide excellent battery life in IoT centric applications.

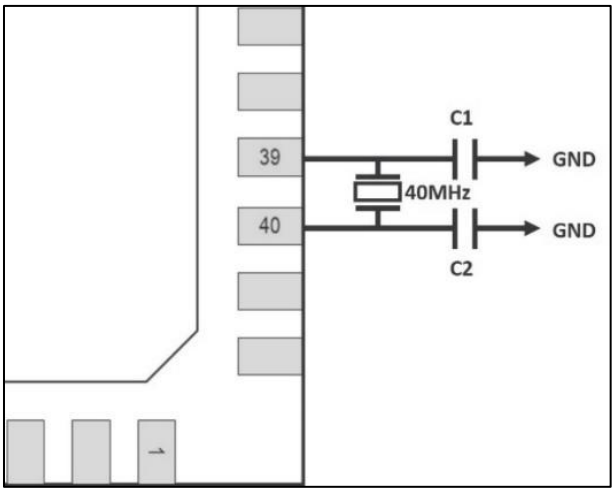


Figure 26: 40MHz Crystal Connections

Parameter (40MHz)	Condition	Min	Typ.	Max	Units
Frequency			40		MHz
Frequency Accuracy	Initial + Temp + Aging	-10		+10	ppm
Load Capacitance		6			pF
Crystal ESR	C1 = C2 = 10pF[1]			60	W

Table 32: Clock conditions and details – 40MHz

Note 1: Recommendation is to choose crystal that uses 10pF capacitors.

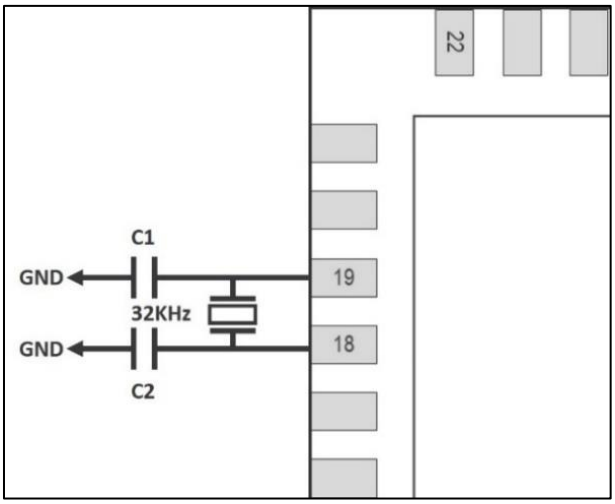


Figure 27: 32kHz Crystal Connections

Parameter (32kHz)	Condition	Min	Typ.	Max	Units
Frequency			32		kHz
Frequency Accuracy	Initial + Temp + Aging	-20		+20	ppm
Load Capacitance			12.5		pF
Crystal ESR	C1 = C2 = 12pF[2]			50k	W

Table 33: Clock conditions and details – 32MHz

INP2045 SoC ESD Ratings

Reliability Test	Standards	Test Conditions	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	+/- 2,000V	PASS[1]

Table 34: INP2045 SoC ESD Ratings

Note: RF Pin HBM = +/- 500V.

INP2045 SoC Chip Reflow Profile

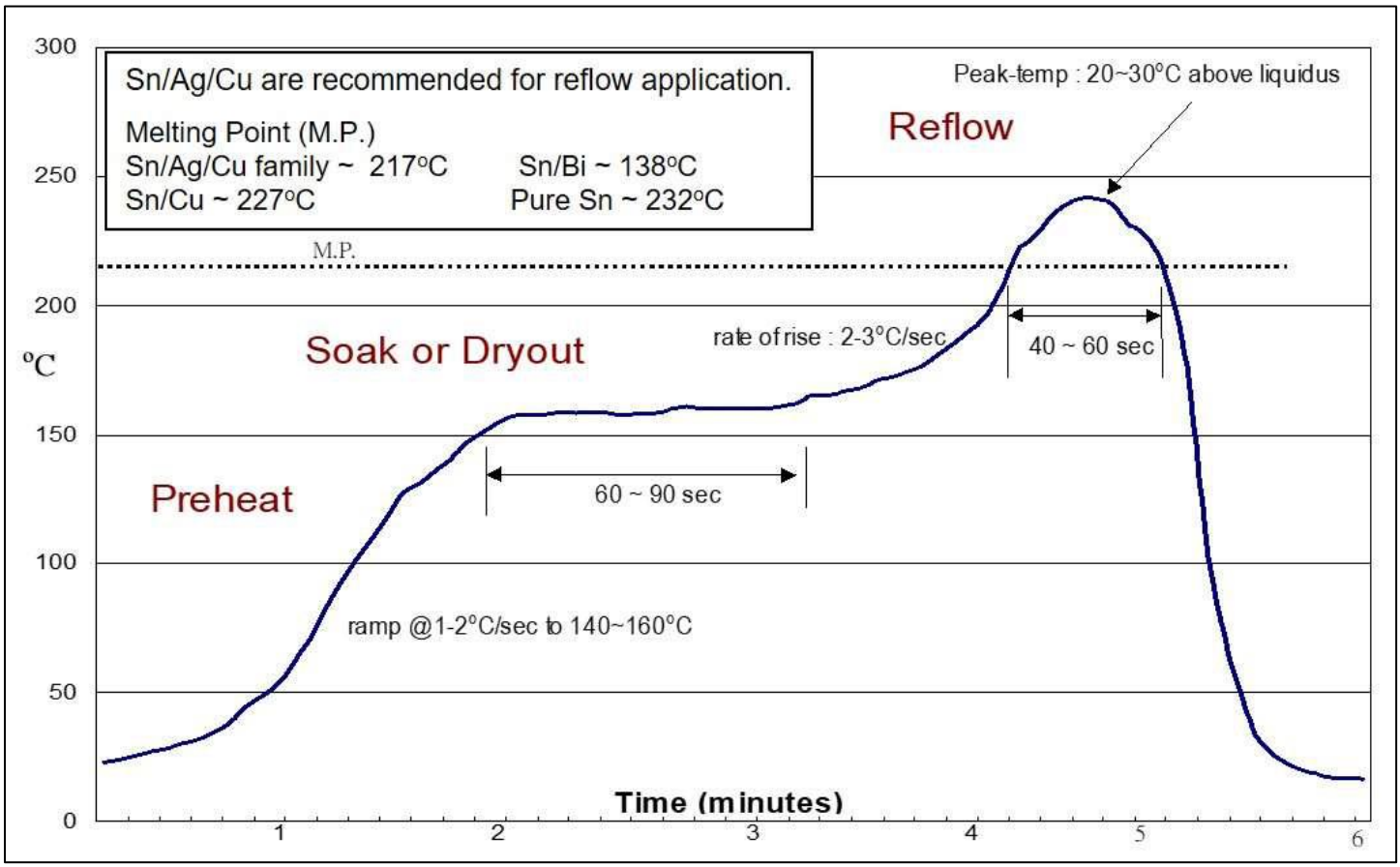
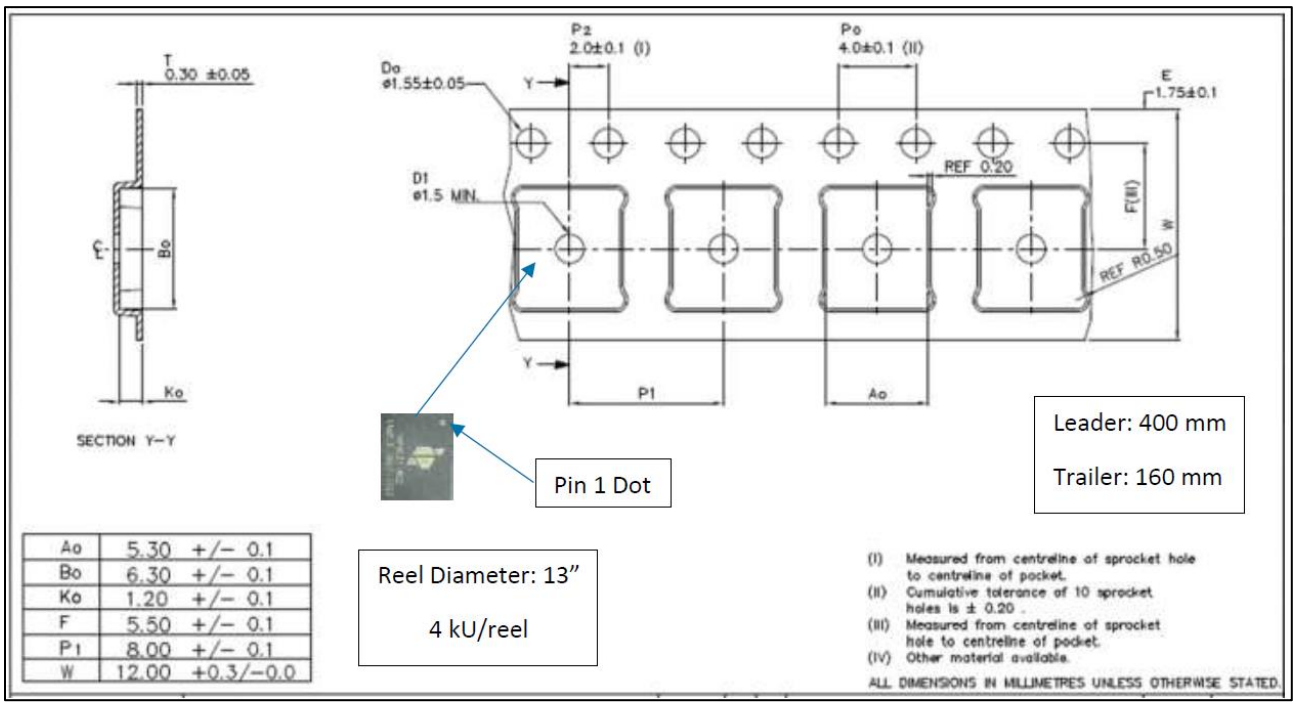


Figure 28: INP2045 SoC Chip Reflow Profile

INP2045 SoC Packing



Ao	5.30	+/– 0.1
Bo	6.30	+/– 0.1
Ko	1.20	+/– 0.1
F	5.50	+/– 0.1
P1	8.00	+/– 0.1
W	12.00	+0.3/–0.0

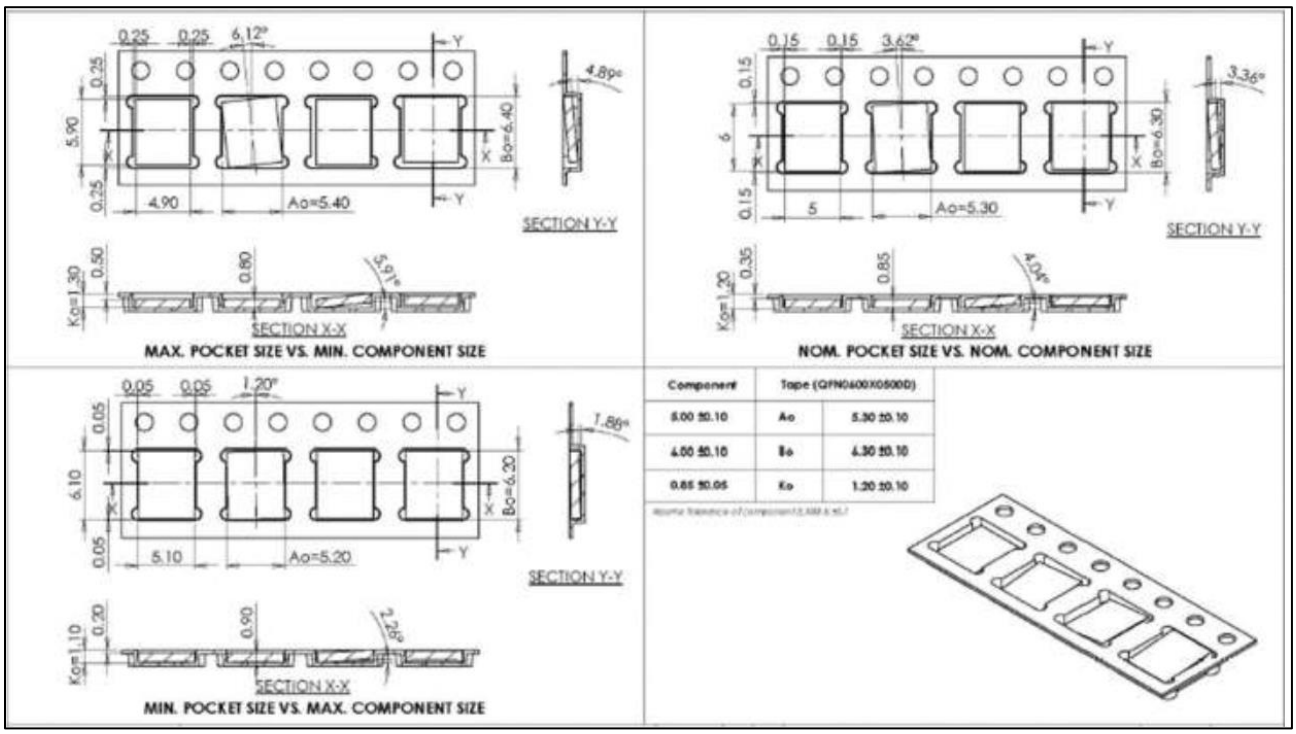


Figure 29: INP2045 SoC Packing

Support

1. Sales Support: Contact an InnoPhase sales representative via email – sales@innophaseiot.com
2. Technical Support:
    a. Visit: https://innophaseiot.com/contact/
    b. Also Visit: https://innophaseiot.com/talaria-two-modules/
    c. Contact: support@innophaseiot.com

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